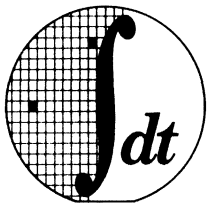

Integrated Device Technology, Inc.

HIGH-SPEED CMOS DATA BOOK

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INTRODUCTION

A major revolution is taking place in the semiconductor industry today. A new technology is rapidly displacing older NMOS and bipolar technologies as the workhorse of the '80s and beyond. That technology is high-speed CMOS. Integrated Device Technology, Inc. is a company totally predicated on and dedicated to implementing high-performance CMOS products to lead this dramatic change.

From our early beginning with the introduction of the industry's fastest CMOS 2Kx8 static RAM, we have grown to a company with three divisions producing a wide range of high-speed CMOS circuits. Our Static RAM Division operates from a new 100,000 square foot facility in Salinas, California, housing an ultra-modern 25,000 square foot clean room, Fab II. The Subsystems Division headquarters, located in Santa Clara, California, houses our advanced vapor phase surface mounting manufacturing line as well as our U.S. monolithic assembly area. The Digital Signal Processing (DSP) Division operates from our corporate headquarters facility, also located in Santa Clara, utilizing its state-of-the-art Fab I clean room.

IDT's goal is to provide you, the user, with a continuing series of high-speed, low-power IC solutions to your system design needs. We hope to make your systems far superior to previous generations in performance, reliability, cost, weight and size.

We are committed to providing you with advanced products produced with leading edge technology. The products in this data book utilize our proprietary technology — CEMOS™ — which employs gate lengths down to 1.2 microns. A more in-depth discussion of our process is presented in the section entitled "Leading Edge CEMOS Technology."

Our commitment, however, extends beyond state-of-the-art technology and advanced products to encompass an exacting reliability and quality level, a factor equally critical to you. All of the military grade products that we manufacture meet or exceed the stringent criteria of the applicable military standard specifications. All IDT products are burned-in and a continuous program of environmental and life-testing per MIL-STD-883, Method 5005 is maintained on each product family. Tables showing military screening flows and quality conformance testing are included following the data sheet pages of this book.

This data book is a snapshot in time of our ever expanding high-speed CMOS product family. Please contact us for an update on our new product introductions.

We are dedicated to delivering these high-quality advanced products to you in a timely manner. If you're producing state-of-the-art equipment, we may be able to help solve some of your problems.

LEADING EDGE CEMOS TECHNOLOGY

CEMOS, the proprietary oxide-isolated silicon-gate technology of Integrated Device Technology, Inc. is the leading edge of new high-speed CMOS processes. Our original CEMOS I process employed 2.5 micron geometries, double-poly construction and dual-well structures. It combined the high packing density of N-channel technology and the greater bus line driveability of bipolar structures with the low power consumption and high-reliability of CMOS devices. The result — the high noise immunity, quiescent power dissipation and wide operating temperature range of CMOS — with speeds comparable to Schottky TTL.

In addition, the dual-well design of CEMOS provides built-in immunity to alpha particles, virtually eliminating induced soft errors. This construction technique also suppresses punch-through and minimizes junction capacitance. The latchup phenomenon of older CMOS processes has been all but eliminated through a combination of careful design layout and proprietary techniques.

Our newest technology—CEMOS II—incorporates all of these same features, but it provides significant performance advances. CEMOS II greatly increases the level of integration possible and provides even faster speeds by reducing gate lengths. (See chart below.) The initial reduction to 2 microns in the CEMOS IIA version of the process was followed by a further scaling to 1.5 microns at the CEMOS IIB level and a final reduction to 1.2 microns with CEMOS IIC.

This aggressive new process utilizes sophisticated processing techniques including direct step on wafer (DSW) alignment printing and dry etching. The basis for the process, however, is the tremendous advantage gained through years of CEMOS I production experience. We consider this to be an invaluable edge over potential competitors who may not have shared the same high-speed CMOS learning curve experiences.

As with CEMOS I, our newest technology is a highly manufacturable production process that does not depend on exotic process techniques or one-of-a-kind wafer fabrication equipment. Readily produceable die sizes are achieved through the use of the fine line geometries and double polysilicon layers.

In general, there is a trend towards smaller, lighter, more trouble-free systems in all applications areas. Our CEMOS products contribute to significantly reducing system size and weight. Reducing power supply costs, eliminating expensive cooling equipment and associated enclosure openings and dust filters through the use of our products could create smaller, lighter, more reliable systems that are more likely to operate maintenance-free for years.

MAINTAINING LEADING-EDGE TECHNOLOGY

The chart below — showing our evolution from the company's original CEMOS I technology to CEMOS II and CEMOS III —depicts the continuous research and development efforts that we expend to maintain our technological leadership in high-speed CMOS.

CEMOS TECHNOLOGY	MINIMUM[1] FEATURE SIZE (MICRONS)	FASTEST SPEED 4Kx4 SRAM COM'L ACCESS TIME (ns)	PRODUCT AVAILABILITY
I	2.5	45	Since 1982
IIA	2.0	35[2]	NOW[2]
IIB	1.5	30	NOW
IIC	1.2	25	NOW
IIIA	1.0	SUB 20	FUTURE

NOTES:

1. There are many claims and counter claims in this area of minimum feature size. We are using here a conservative approach, i.e. the gate length as physically measured on a scanning electron microscope.
2. Estimate — not manufactured in CEMOS IIA. Our 4Kx4 static RAM is used as a typical product to illustrate the figures of merit of this constant drive for ever higher performance standards.

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SELECTOR GUIDE

IDT HIGH-SPEED STATIC RAM SELECTOR GUIDE

PART NUMBER	ORGANIZATION	MAXIMUM SPEEDS (NS) MIL	MAXIMUM SPEEDS (NS) COM'L	POWER (TYP) OPER	POWER (TYP) STANDBY	PACKAGE	FEATURE/AVAILABILITY
HIGH-SPEED STATIC RAMS IDT7198 64K	16K x 4	45	45	300mW	30μW	24-Pin THINDIP, 28-Pin LCC	• Output Enable ($\overline{OE}$) pin available for added system flexibility • Multiple chip selects ($\overline{CS}_1$, $\overline{CS}_2$) simplify system design and operation • Available now
IDT7188 64K	16K x 4	45	45	300mW	30μW	22-Pin DIP	• Industry standard pinout • Available now
IDT7187 64K	64K x 1	45	35	250mW	30μW	22-Pin DIP, 28-Pin LCC	• Industry standard pinouts • Available now
IDT7164 64K	8K x 8	70	55	250mW	30μW	28-Pin DIP, 32-Pin LCC	• Industry standard pinouts • Available 4Q85
IDT6116 16K	2K x 8	55	55	160mW	20μW	24-Pin THINDIP, 24-Pin DIP, 28-& 32-Pin LCC, 24-Lead Flatpack	• Chip select access time of 50ns • Available now
IDT71681A/82A IDT71681/82 16K	4K x 4	35 55	25 45	225mW 225mW	10μW 10μW	24-Pin THINDIP, 28-Pin LCC	• Separate data inputs and outputs • IDT71681 outputs track inputs during write mode • IDT71682 high impedance during write mode • Available now
IDT6168A IDT6168 16K	4K x 4	35 55	25 45	225mW 225mW	10μW 10μW	20-Pin DIP, 20-Pin LCC, 20-Lead Flatpack	• Bidirectional data input and output • Available now
IDT6167A IDT6167 16K	16K x 1	35 55	25 45	200mW 125mW	10μW 10μW	20-Pin DIP, 20-Pin LCC, 20-Lead Flatpack	• Separate data input and output • 55ns mil. and 45ns com'l available now • 35ns mil. and 25ns com'l available 3Q85
DUAL PORT RAMS IDT7132 16K	2K x 8	100	90	325mW	1mW	48-Pin DIP, 48-Pin LCC	• On-chip arbitration logic • Fully asynchronous operation from either port • Available now
IDT7130 8K	1K x 8	100	90	325mW	1mW	48-Pin DIP, 48-Pin LCC	• On-chip arbitration logic • Fully asynchronous operation from either port • Available now

NOTE:
1. All IDT static RAMS have 2V data retention battery backup.

SELECTOR GUIDE

IDT HIGH-SPEED CMOS DIGITAL SIGNAL PROCESSING SELECTOR GUIDE

PART NUMBER	ORGANIZATION	INDUSTRY STANDARD EQUIV.	PACKAGE TYPE	SPEED (MAX ns)		I_{CC} (MAX mA)		STANDBY CURRENT (MAX mA)		FEATURE
				COM'L	MIL	COM'L	MIL	COM'L	MIL	
IDT7216	16 x 16 Multiplier	AM 29516 MPY016H/K	64-PIN DIP 68-PIN LCC 64-LEAD FLATPACK	55 65 75 90 140	70 75 90 120 185	80 60	100 80	20 1	25 2	• IDT7216 has separate input and output clock signals • User-controlled option for transparent output register mode
IDT7217	16 x 16 Multiplier with single clock architecture	AM29517	64-PIN DIP 68-PIN LCC 64-LEAD FLATPACK	55 65 75 90 140	70 75 90 120 185	80 60	100 80	20 1	25 2	• IDT7217 has single clock input and separate register enables • Three separate register enables for inputs and outputs
IDT7201	512x9 FIFO with half-full flag	MK4501	28-PIN DIP 32-PIN LCC	50 65 80 120	50 65 80 120	80	100	0.5	0.9	• Empty, full and half-full flags indicate FIFO status
IDT7202	1024x9 FIFO with half-full flag	Proprietary	28-PIN DIP 32-PIN LCC	50 65 80 120	50 65 80 120	80	100	0.5	0.9	• Fully expandable by word-width and depth • Retransmit pin to reread data beginning at first location
IDT7210	16 x 16 Multiplier/ Accumulator with 35-bit output	TDC1010	64-PIN DIP 68-PIN LCC	65 75 100 165	75 85 120 200	120 110	140 130	20 1	25 2	• Full 35-bit product output • Selectable accumulation, subtraction and rounding
IDT7243	16 x 16 Multiplier/ Accumulator with 19-bit output	TDC1043	64-PIN DIP 68-PIN LCC	65 75 100 165	75 85 120 200	120 110	140 130	20 1	25 2	• 19-bit most significant product output • Fully de-multiplexed inputs and outputs
IDT7212	12 x 12 Multiplier	MPY012H	64-PIN DIP 68-PIN LCC 64-LEAD FLATPACK	45 70 115	55 90 140	80 60	100 80	20 1	25 2	• User-controlled round and transparent output mode • Fully de-multiplexed inputs and outputs for single cycle output
IDT7213	12 x 12 Multiplier with single clock architecture	Proprietary	64-PIN DIP 68-PIN LCC 64-LEAD FLATPACK	45 70 115	55 90 140	80 60	100 80	20 1	25 2	• Three separate register enables for inputs and outputs • Format adjust control for two's complement arithmetic
IDT7209	12 x 12 Multiplier/ Accumulator	TDC1009	64-PIN DIP 68-PIN LCC	55 65 100 135	65 75 120 170	120 110	140 130	20 1	25 2	• Performs subtraction and double precision addition and multiplication • Selectable accumulation, subtraction, rounding, and preloading with 27-bit result

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SELECTOR GUIDE

IDT HIGH-SPEED CMOS MEMORY INTERFACE SELECTOR GUIDE

PART NUMBER	DESCRIPTION	PACKAGE TYPE	SPEED (ns) COM'L		SPEED (ns) MIL		I_{CC} (Max. mA) 10MHz (FCT)		STANDBY I_{CCQ} (Max. mA)		FEATURES
			TYP.	MAX.	TYP.	MAX.	COM'L	MIL	COM'L	MIL	
IDT54/74 FCT374	FAST™ CMOS Octal D Flip Flop	20-Pin DIP 20-Pin LCC	6.5	10.0	6.5	11.0	4.5	4.5	2.0	2.0	Same speed and output drive as FAST™, but at CMOS power.
IDT54/74 FCT273	FAST™ CMOS Octal D Flip Flop	20-Pin DIP 20-Pin LCC	7.0	—	7.0	—	—	—	2.0	2.0	Same speed and output drive as FAST™, but at CMOS power.
IDT54/74 FCT299	FAST™ CMOS Octal Universal Shift Register	20-Pin DIP 20-Pin LCC	7.0	10.0	7.0	—	—	—	2.0	2.0	Same speed and output drive as FAST™, but at CMOS power.
IDT54/74 FCT377	FAST™ CMOS Octal D Flip-Flop	20-Pin DIP 20-Pin LCC	7.0	—	7.0	—	—	—	2.0	2.0	Same speed and output drive as FAST™, but at CMOS power.
IDT54/74 FCT534	FAST™ CMOS Octal D Flip-Flop	20-Pin DIP 20-Pin LCC	6.5	10.0	6.5	11.0	4.5	4.5	2.0	2.0	Same speed and output drive as FAST™, but at CMOS power.
IDT54/74 FCT373	FAST™ CMOS Octal Transparent Latch	20-Pin DIP 20-Pin LCC	5.0	8.0	5.0	8.5	4.5	4.5	2.0	2.0	Same speed and output drive as FAST™, but at CMOS power.
IDT54/74 FCT533	FAST™ CMOS Octal Transparent Latch	20-Pin DIP 20-Pin LCC	6.0	10.0	6.0	12.0	4.5	4.5	2.0	2.0	Same speed and output drive as FAST™, but at CMOS power.
IDT54/74 FCT240	FAST™ CMOS Octal Buffer	20-Pin DIP 20-Pin LCC	5.0	8.0	5.0	9.0	4.5	4.5	2.0	2.0	Same speed and output drive as FAST™, but at CMOS power.
IDT54/74 FCT244	FAST™ CMOS Octal Buffer	20-Pin DIP 20-Pin LCC	4.5	6.5	4.5	7.0	4.5	4.5	2.0	2.0	Same speed and output drive as FAST™, but at CMOS power.
IDT54/74 FCT245	FAST™ CMOS Octal Bi-directional Transceiver	20-Pin DIP 20-Pin LCC	5.0	7.0	5.0	7.5	4.5	4.5	2.0	2.0	Same speed and output drive as FAST™, but at CMOS power.
IDT54/74 FCT645	FAST™ CMOS Octal Bi-directional Transceiver	20-Pin DIP 20-Pin LCC	6.0	9.5	6.0	11.0	4.5	4.5	2.0	2.0	Same speed and output drive as FAST™, but at CMOS power.
IDT54/74 FCT640	FAST™ CMOS Octal Bi-directional Transceiver	20-Pin DIP 20-Pin LCC	6.0	7.0	6.0	8.0	4.5	4.5	2.0	2.0	Same speed and output drive as FAST™, but at CMOS power.
IDT54/74 FCT138	FAST™ CMOS 1-of-8 Decoder	16-Pin DIP 20-Pin LCC	7.0	9.0	7.0	12.0	5.0	5.0	2.0	2.0	Same speed and output drive as FAST™, but at CMOS power.
IDT54/74 FCT139	FAST™ CMOS Dual 1-of-4 Decoder	16-Pin DIP 20-Pin LCC	6.0	9.0	6.0	12.0	5.0	5.0	2.0	2.0	Same speed and output drive as FAST™, but at CMOS power.
IDT54/74 FCT521	FAST™ CMOS 8-bit Comparator	20-Pin DIP 20-Pin LCC	7.0	11.0	7.0	15.0	—	—	2.0	2.0	Same speed and output drive as FAST™, but at CMOS power.
IDT54/74 AHCT374	High-Speed CMOS Octal D Flip-Flop	20-Pin DIP 20-Pin LCC	10.0	16.0	10.0	18.0	2.3	2.3	2.0	2.0	Same speed and output drive as ALS, but at CMOS power.
IDT54/74 AHCT273	High-Speed CMOS Octal D Flip-Flop	20-Pin DIP 20-Pin LCC	10.0	15.0	10.0	17.0	2.3	2.3	2.0	2.0	Same speed and output drive as ALS, but at CMOS power.
IDT54/74 AHCT299	High-Speed CMOS Universal Shift Register	20-Pin DIP 20-Pin LCC	9.0	—	9.0	—	—	—	—	—	Same speed and output drive as ALS, but at CMOS power.
IDT54/74 AHCT377	High-Speed CMOS Octal D Flip-Flop	20-Pin DIP 20-Pin LCC	7.0	—	7.0	—	—	—	2.0	2.0	Same speed and output drive as ALS, but at CMOS power.
IDT54/74 AHCT534	High-Speed CMOS Octal D Flip-Flop	20-Pin DIP 20-Pin LCC	10.0	16.0	10.0	18.0	2.3	2.3	2.0	2.0	Same speed and output drive as ALS, but at CMOS power.
IDT54/74 AHCT373	High-Speed CMOS Octal Transparent Latch	20-Pin DIP 20-Pin LCC	10.0	16.0	10.0	19.0	2.3	2.3	2.0	2.0	Same speed and output drive as ALS, but at CMOS power.
IDT54/74 AHCT533	High-Speed CMOS Octal Transparent Latch	20-Pin DIP 20-Pin LCC	11.0	19.0	11.0	24.0	2.3	2.3	2.0	2.0	Same speed and output drive as ALS, but at CMOS power.
IDT54/74 AHCT240	High-Speed CMOS Octal Buffer	20-Pin DIP 20-Pin LCC	7.0	9.0	7.0	12.0	2.3	2.3	2.0	2.0	Same speed and output drive as ALS, but at CMOS power.
IDT54/74 AHCT244	High-Speed CMOS Octal Buffer	20-Pin DIP 20-Pin LCC	7.0	10.0	7.0	13.0	2.3	2.3	2.0	2.0	Same speed and output drive as ALS, but at CMOS power.

FAST is a trademark of Fairchild Camera and Instrument.

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SELECTOR GUIDE

IDT HIGH-SPEED CMOS MEMORY INTERFACE SELECTOR GUIDE

PART NUMBER	DESCRIPTION	PACKAGE TYPE	SPEED (ns) COM'L		SPEED (ns) MIL		I_{CC} (Max. mA) 10MHz (FCT)		STANDBY I_{CCQ} (Max. mA)		FEATURES
			TYP.	MAX.	TYP.	MAX.	COM'L	MIL	COM'L	MIL	
IDT54/74 AHCT245	High-Speed CMOS Octal Bi-Directional Transceiver	20-Pin DIP 20-Pin LCC	8.0	10.0	8.0	15.0	2.3	2.3	2.0	2.0	Same speed and output drive as ALS, but at CMOS power.
IDT54/74 AHCT645	High-Speed CMOS Octal Bi-Directional Transceiver	20-Pin DIP 20-Pin LCC	8.0	10.0	8.0	15.0	2.3	2.3	2.0	2.0	Same speed and output drive as ALS, but at CMOS power.
IDT54/74 AHCT640	High-Speed CMOS Octal Bi-Directional Transceiver	20-Pin DIP 20-Pin LCC	10.0	11.0	10.0	14.0	4.5	4.5	2.0	2.0	Same speed and output drive as ALS, but at CMOS power.
IDT54/74 AHCT138	High-Speed CMOS 1-of-8 Decoder	16-Pin DIP 20-Pin LCC	11.0	22.0	11.0	27.0	2.3	2.3	2.0	2.0	Same speed and output drive as ALS, but at CMOS power.
IDT54/74 AHCT139	High-Speed CMOS Dual 1-of-4 Decoder	16-Pin DIP 20-Pin LCC	9.0	20.0	9.0	25.0	2.3	2.3	2.0	2.0	Same speed and output drive as ALS, but at CMOS power.
IDT54/74 AHCT521	High-Speed CMOS 8-bit Comparator	20-Pin DIP 20-Pin LCC	9.0	—	9.0	—	—	—	2.0	2.0	Same speed and output drive as ALS, but at CMOS power.

Integrated Device Technology, Inc.

SELECTOR GUIDE

IDT HIGH-SPEED CMOS MODULE SELECTOR GUIDE

PART NUMBER	DESCRIPTION	ORGANI-ZATION	PACKAGE TYPE	I_{CC} (MAX mA) COM'L/MIL	I_{SB1} STANDBY (MAX mA) COM'L	I_{SB1} STANDBY (MAX mA) MIL	ACCESS TIME (MAX ns) COM'L	ACCESS TIME (MAX ns) MIL	FEATURES
IDT7M164	64K CMOS Static RAMPAK	64K x 1	.300 WIDE 22-PIN DIP	110	1.0	3.6	60 70 100 120	70 85 100	• Static RAM Pinout
IDT7M464	64K CMOS Static RAMPAK	16K x 4	.300 WIDE 22-PIN DIP	200	1.0	3.6	55 65 85	65 85 100	• Static RAM Pinout
IDT8M464	64K CMOS Static RAMPAK	16K x 4	.400 WIDE 22-PIN DIP	200	1.0	3.6	55 65 85	65 85 100	• Low Profile Package
IDT7M864	64K CMOS Static RAMPAK	8K x 8	.600 WIDE 28-PIN DIP	180	1.0	3.6	65 75 85 120 150 200	75 85 120 150 200	• Static RAM Pinout
IDT8M864	64K CMOS Static RAMPAK	8K x 8	.600 WIDE 28-PIN DIP	180	1.0	3.6	65 75 85 120 150 200	75 85 120 150 200	• EPROM Pinout
IDT7M856	256K CMOS Static RAMPAK	32K x 8	.600 WIDE 28-PIN DIP	360	12.0	12.0	60 70 80	75 90 100	• Static RAM Pinout
IDT7M656	256K CMOS Static RAMPAK	16K x 16 32K x 8 64K x4	.900 WIDE 40-PIN DIP	440	5.0	15.0	55 65 85	65 85 100	• Customer configurable organization
IDT7M624	1 Megabit CMOS Static RAMPAK	64K x 16 128K x 8 256K x 4	.900 WIDE 40-PIN DIP	—	—	—	55 65 85	65 85 100	• Customer configurable organization
IDT7M203	16K CMOS FIFO Module	2K x 9	.600 WIDE 28-PIN DIP	176/230	2.0	3.6	65 100 140	65 100 140	• Pin compatible with 512 x 9 and 1K x9 FIFOs
IDT7M204	32K CMOS FIFO Module	4K x 9	.600 WIDE 28-PIN DIP	176/230	2.0	3.6	65 100 140	65 100 140	• Pin compatible with 512 x 9 and 1K x9 FIFOs
IDT7M812	512K CMOS Static RAMPAK	64K x 8	.600 WIDE 40-PIN DIP	—	—	—	—	—	• Maximum addressable memory of 8-bit up
IDT7M912	512K CMOS Static RAMPAK	64K x 9	.600 WIDE 40-PIN DIP	—	—	—	—	—	• Maximum addressable memory of 8-bit up
IDT7M134	64K CMOS Dual Port RAM Module	8K x 8	.600 WIDE 58-PIN DIP	—	—	—	115	125	• Fully asynchronous operation from either port
IDT7M135	128K CMOS Dual Port RAM Module	16K x 8	.600 WIDE 58-PIN DIP	—	—	—	115	125	• Largest Dual Port RAM available

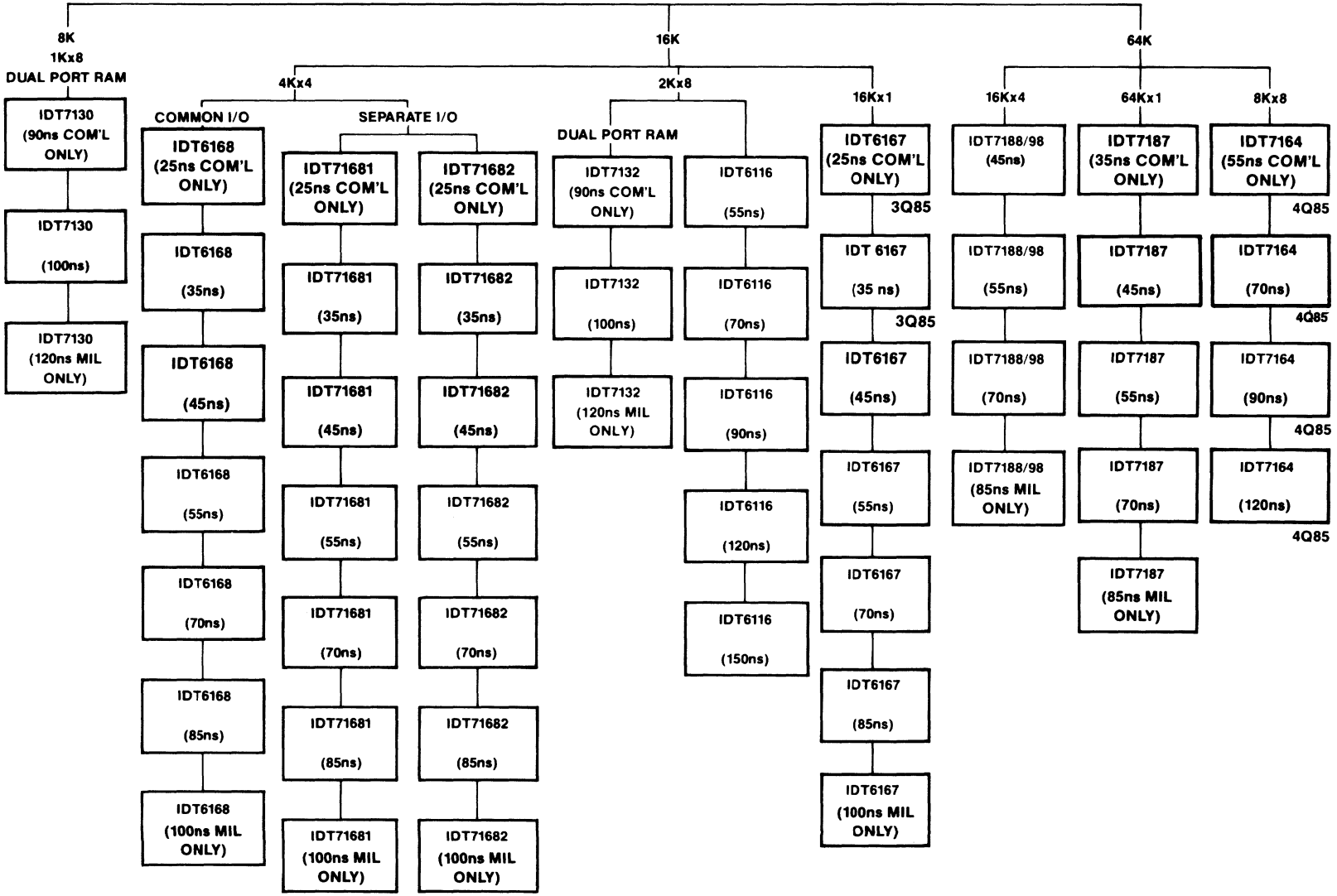
HIGH-SPEED CMOS STATIC RAM PRODUCTS

CONTENTS **PAGE**

Integrated Device Technology, Inc.

LEADING THE CMOS FUTURE

CEMOS™ STATIC RAMs



*Dates represent sample availability.

CEMOS is a trademark of Integrated Device Technology, Inc.

CMOS STATIC RAMS 16K (16K × 1 BIT)

ADVANCE INFORMATION
IDT6167SA
IDT6167LA

FEATURES:

- High-speed (equal access and cycle time)
  - —Military/Industrial—35/45ns (max.)
  - —Commercial—25/35ns (max.)
- Low power consumption
  - —IDT6167SA
    - Active: 250mW (typ.)
    - Standby: 100μW (typ.)
  - —IDT6167LA
    - Active: 200mW (typ.)
    - Standby: 10μW (typ.)
- Battery backup operation—2V data retention voltage (IDT6167L only)
- High-density 20-pin dual in-line package and 20-pin leadless chip carriers
- Produced with advanced CEMOS™ high-performance technology
- Separate data input and output
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Pin-compatible with standard 16K × 1 static RAMs
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT6167 is a 16,384-bit high-speed static RAM organized as 16K x 1. It is fabricated using IDT's high-performance, high reliability technology—CEMOS™. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

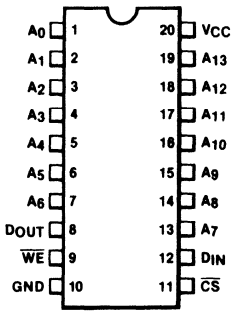
Access times as fast as 25ns are available with maximum power consumption of only 440mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode. In the standby mode, the device consumes less than 10μW, typically. This capability provides significant system-level power and cooling savings. The low power, (L), version also offers a battery backup data retention capability where the circuit typically consumes only 1μW operating off of a 2V battery.

All inputs and the output of the IDT6167 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

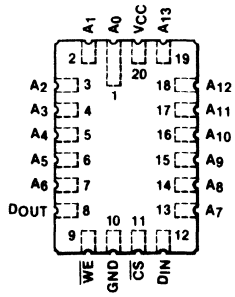
The IDT6167 is packaged in either a space-saving 20-pin, 300 mil DIP or 20-pin leadless chip carrier, providing high board-level packing densities.

The IDT6167 Military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS

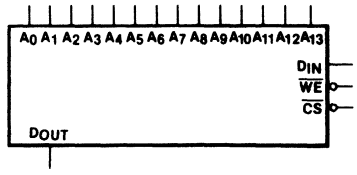


DIP
TOP VIEW

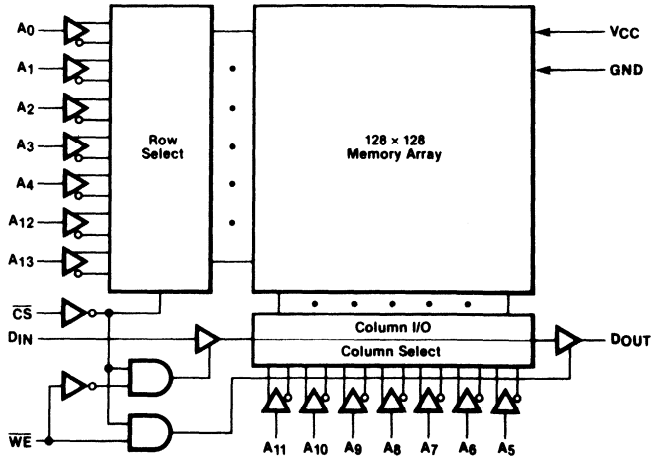


LCC
TOP VIEW

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0-A_{13}	ADDRESS INPUTS	D_{IN}	DATA IN
$\overline{CS}$	CHIP SELECT	D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE	GND	GROUND
V_{CC}	POWER		

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Integrated Device Technology, Inc.

CMOS STATIC RAMS 16K (16K x 1 BIT)

IDT6167S
IDT6167L

FEATURES:

- High-speed (equal access and cycle time)
  - —Military/Industrial-55/70/85/100ns (max.)
  - —Commercial-45/55/70/85ns (max.)
- Low power consumption
  - —IDT6167S
    - Active: 150mW (typ.)
    - Standby: 100μW (typ.)
  - —IDT6167L
    - Active: 125mW (typ.)
    - Standby: 10μW (typ.)
- Battery backup operation — 2V data retention voltage (IDT6167L only)
- High-density 20-pin dual-in-line package and 20-pin leadless chip carriers
- Produced with advanced CEMOS™ I high-performance technology
- CEMOS™ I process virtually eliminates alpha particle soft-error rates (with no organic die coatings)
- Separate data input and output
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Pin-compatible with standard 16K x 1 static RAMs
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT6167 is a 16,384-bit high-speed static RAM organized as 16K x 1. It is fabricated using IDT's high-performance, high-reliability technology — CEMOS™ I. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

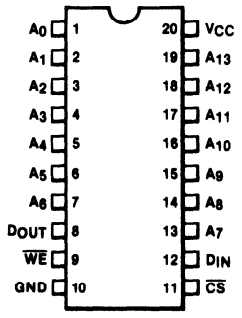
Access times as fast as 55ns are available with maximum power consumption of only 330mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consumes less than 100μW, typically. This capability provides significant system-level power and cooling savings. The low power, (L), version also offers a battery backup data retention capability where the circuit typically consumes only 1μW operating off of a 2V battery.

All inputs and the output of the IDT6167 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT6167 is packaged in either a space-saving 20-pin, 300 mil DIP or 20-pin leadless chip carrier, providing high board-level packing densities.

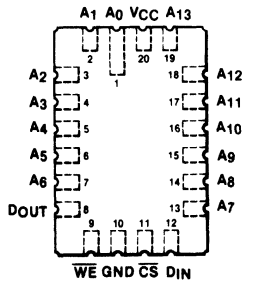
The IDT6167 Military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



SRD6167-001

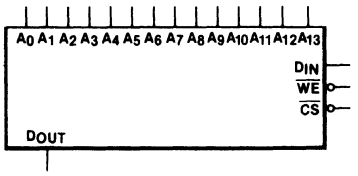
DIP
TOP VIEW



SRD6167-002

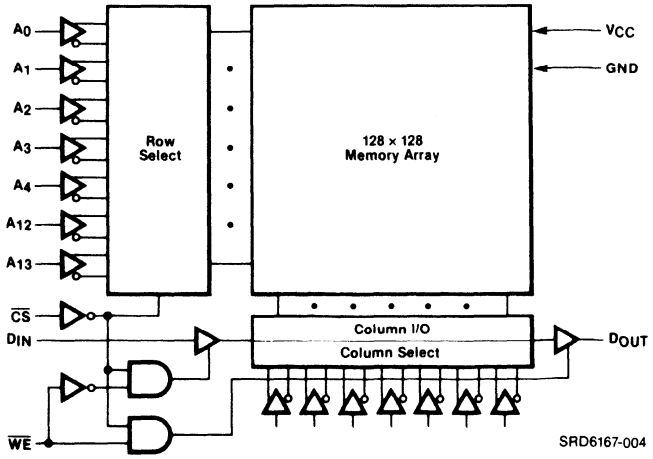
LCC
TOP VIEW

LOGIC SYMBOL



SRD6167-003

FUNCTIONAL BLOCK DIAGRAM



SRD6167-004

PIN NAMES

A_0-A_{13}	ADDRESS INPUTS	D_{IN}	DATA IN
$\overline{CS}$	CHIP SELECT	D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE	GND	GROUND
V_{CC}	POWER		

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MILITARY, INDUSTRIAL, AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING		VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND		-0.5 to +7.0	V
T_A	Operating Temperature	COML. IND. MIL.	0 to +70 -40 to +85 -55 to +125	°C
T_{BIAS}	Temperature Under Bias		-65 to +135	°C
T_{STG}	Storage Temperature		-65 to +150	°C
P_T	Power Dissipation		1.0	W
I_{OUT}	DC Output Current		50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20 ns.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5.0V ± 10%, $V_{CC(min.)}$ = 4.5V, $V_{CC(max.)}$ = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT6167S MIN.	IDT6167S TYP.(1)	IDT6167S MAX.	IDT6167L MIN.	IDT6167L TYP.(1)	IDT6167L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL. IND. COM'L.	— — —	— — —	10 10 2	— — —	— — —	5 2 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. CS = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. IND. COM'L.	— — —	— — —	10 10 2	— — —	— — —	5 2 2	µA
I_{CC1}	Operating Power Supply Current	CS = V_{IL}, Output Open V_{CC} = Max.	MIL. IND. COM'L.	— — —	30 30 30	60 60 60	— — —	25 25 25	50 50 50	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100% V_{CC} = Max., Output Open	MIL. IND. COM'L.	— — —	30 30 30	60 60 60	— — —	25 25 25	50 50 50	mA
I_{SB}	Standby Power Supply Current	CS ≥ V_{IH} V_{CC} = Max. Min. Duty Cycle = 100%	MIL. IND. COM'L.	— — —	5 5 5	20 20 20	— — —	5 5 5	20 20 20	mA
I_{SB1}	Full Standby Power Supply Current	CS ≥ V_{HC}, V_{CC} = Max. V_{IN} ≥ V_{HC} or ≤ V_{LC}	MIL. IND. COM'L.	— — —	.02 .02 .02	10 10 2	— — —	.002 .002 .002	.9 .15 .05	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA V_{CC} = Min.		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA V_{CC} = Min.		2.4	—	—	2.4	—	—	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

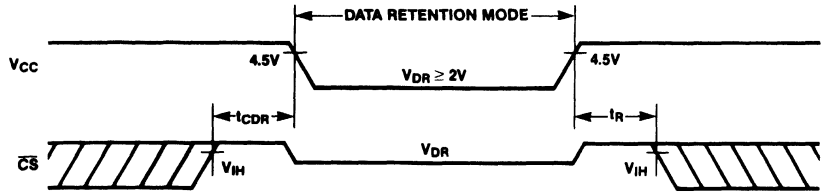
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC}@ 2.0V	TYP.(1) V_{CC}@ 3.0V	MAX. V_{CC}@ 2.0V	MAX. V_{CC}@ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	—	—	2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	CS ≥ V_{HC} V_{IN} ≥ V_{HC} or ≤ V_{LC}	MIL. IND. COM'L.	— — —	.5 .5 .5	1.0 1.0 1.0	300 40 20	450 60 30	µA
t_{CDR}	Chip Deselect to Data Retention Time			0			—		ns
t_R	Operation Recovery Time			t_{RC}(2)	—		—		ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—		2		µA

NOTES:

1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

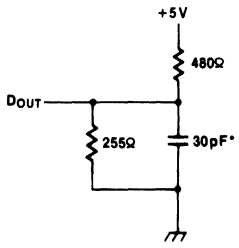


Figure 1. Output Load

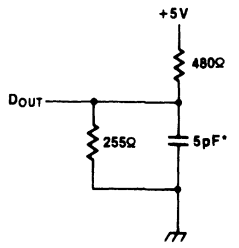


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and -40°C to +85°C)

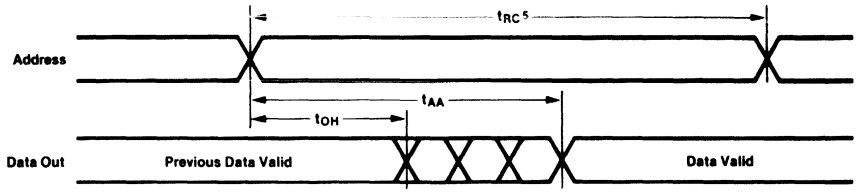
SYMBOL	PARAMETER	IDT6167S55 IDT6167L55 MIN.	MAX.	IDT6167S70 IDT6167L70 MIN.	MAX.	IDT6167S85 IDT6167L85 MIN.	MAX.	IDT6167S100 IDT6167L100 MIN.	MAX.	UNIT
READ CYCLE										
t_{RC} (TAVAV)	Read Cycle Time	55	—	70	—	85	—	100	—	ns
t_{AA} (TAVQV)	Address Access Time	—	55	—	70	—	85	—	100	ns
t_{ACS} (TELQV)	Chip Select Access Time	—	55	—	70	—	85	—	100	ns
t_{OH} (TAXQX)	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{LZ} (TELQX) (1)	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{HZ} (TEHQZ) (1)	Chip Deselection to Output in High Z	0	40	0	40	0	50	0	50	ns
t_{PU} (TELICCH) (1)	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD} (TEHICCL) (1)	Chip Deselection to Power Down Time	—	55	—	70	—	85	—	100	ns
WRITE CYCLE										
t_{WC} (TAVAV)	Write Cycle Time	55	—	70	—	85	—	100	—	ns
t_{CW} (TELWH)	Chip Selection to End of Write	45	—	55	—	65	—	80	—	ns
t_{AW} (TAVWH)	Address Valid to End of Write	45	—	55	—	65	—	80	—	ns
t_{AS} (TAVWL)	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WP} (TWLWH)	Write Pulse Width	35	—	40	—	45	—	55	—	ns
t_{WR} (TWHAX)	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW} (TDVWH)	Data Valid to End of Write	25	—	30	—	35	—	40	—	ns
t_{DH} (TWHDX)	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WZ} (TWLQZ) (1)	Write Enable to Output in High Z	0	40	0	40	0	50	0	50	ns
t_{OW} (TWHQZ) (1)	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0 to 70°C)

SYMBOL	PARAMETER	IDT6167S45 IDT6167L45 MIN.	MAX.	IDT6167S55 IDT6167L55 MIN.	MAX.	IDT6167S70 IDT6167L70 MIN.	MAX.	IDT6167S85 IDT6167L85 MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	45	—	55	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	—	85	ns
t_{ACS}	Chip Select Access Time	—	45	—	55	—	70	—	85	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{LZ} (1)	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{HZ} (1)	Chip Deselection to Output in High Z	0	30	0	30	0	30	0	40	ns
t_{PU} (1)	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD} (1)	Chip Deselection to Power Down Time	—	35	—	35	—	35	—	40	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	45	—	55	—	70	—	85	—	ns
t_{CW}	Chip Selection to End of Write	40	—	45	—	55	—	65	—	ns
t_{AW}	Address Valid to End of Write	40	—	45	—	55	—	65	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	30	—	35	—	40	—	45	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	25	—	25	—	30	—	35	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WZ} (1)	Write Enable to Output in High Z	0	30	0	30	0	30	0	40	ns
t_{OW} (1)	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

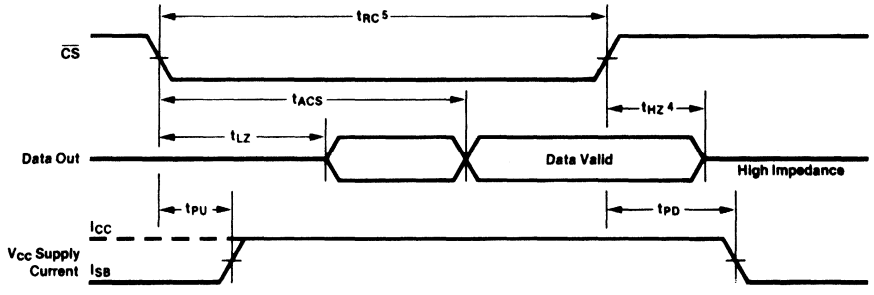
NOTE:
1. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1,2)



SRD6167-008

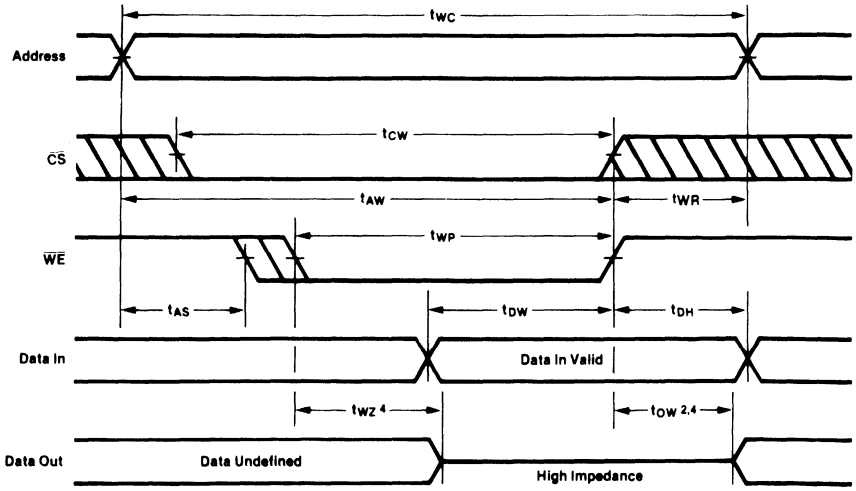
TIMING WAVEFORM OF READ CYCLE NO. 2(1,3)



SRD6167-009

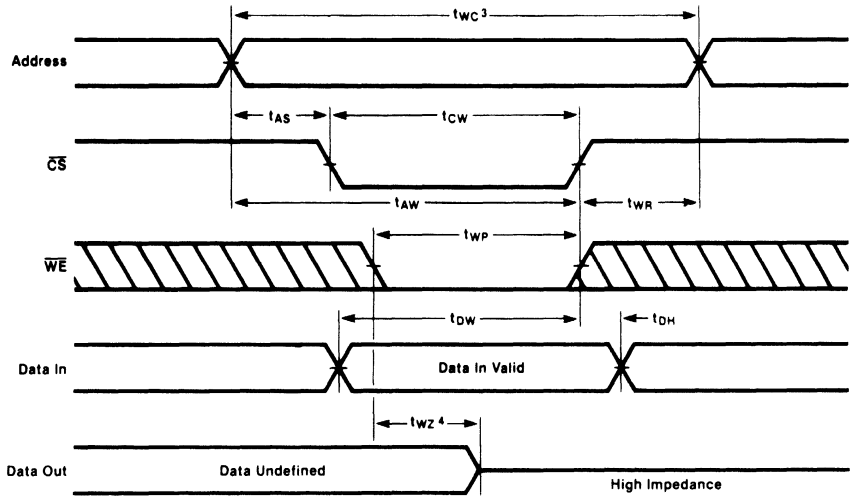
NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1]



SRD6167-010

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1]



SRD6167-011

NOTES: 1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

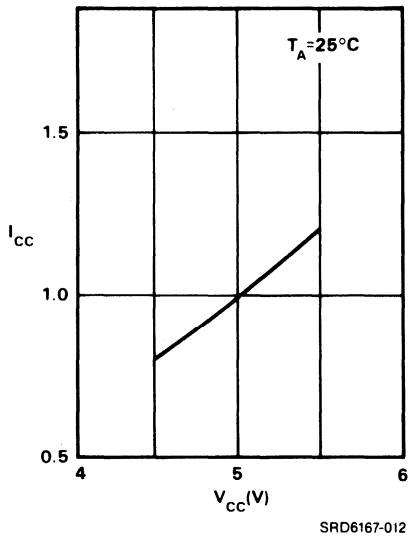
CAPACITANCE (T_A = 25°C, f = 1.0MHz)

SYMBOL	ITEM	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	6	pF

NOTE: This parameter is sampled and not 100% tested.

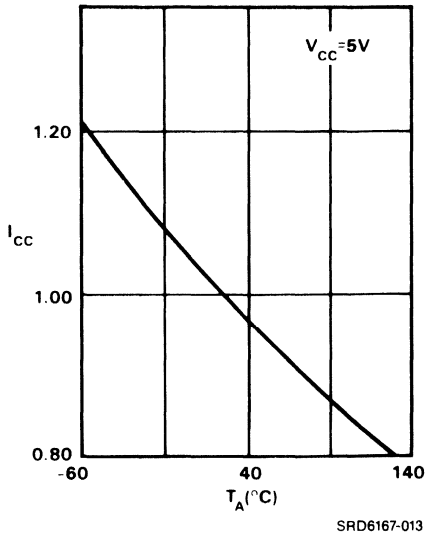
NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

I_{CC} vs. Supply Voltage



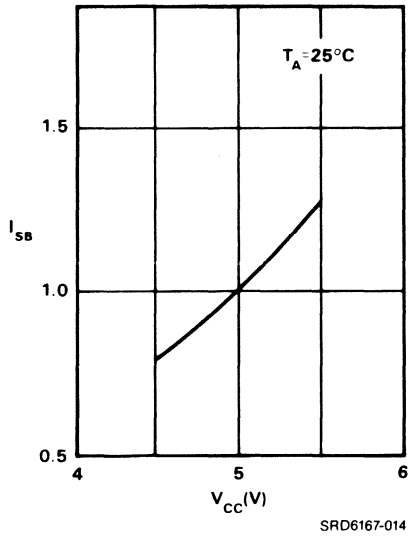
SRD6167-012

I_{CC} vs. Temperature



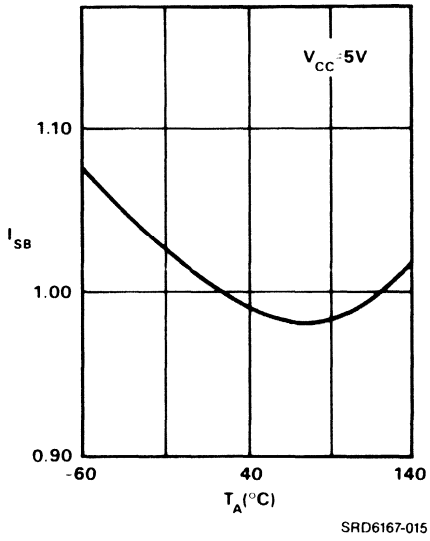
SRD6167-013

I_{SB} vs. Supply Voltage



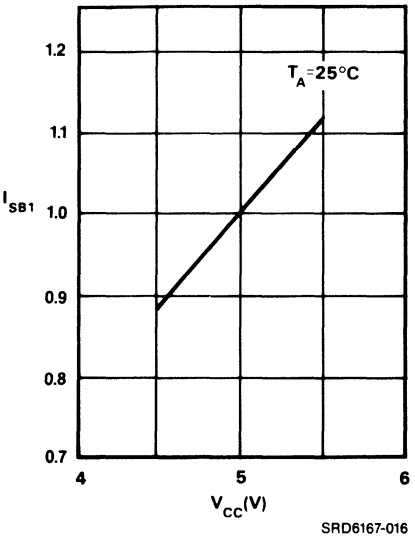
SRD6167-014

I_{SB} vs. Temperature



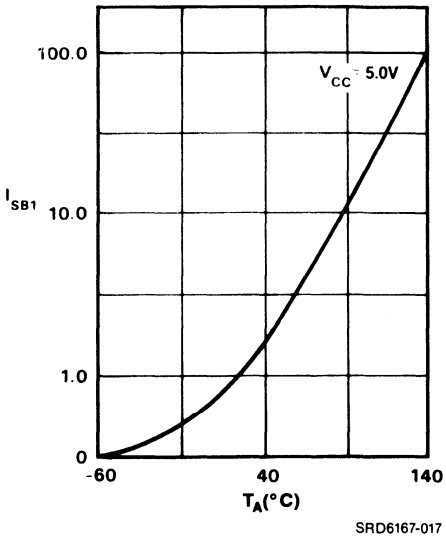
SRD6167-015

I_{SB1} vs. Supply Voltage



SRD6167-016

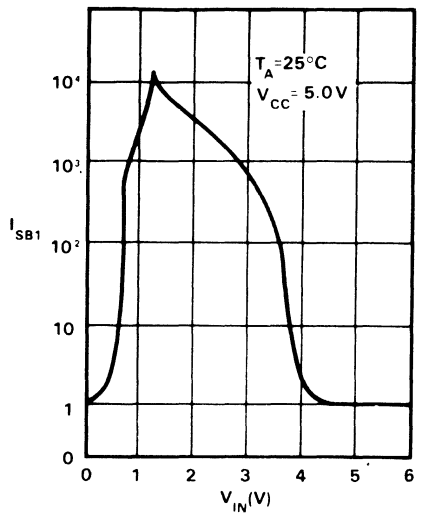
I_{SB1} vs. Temperature



SRD6167-017

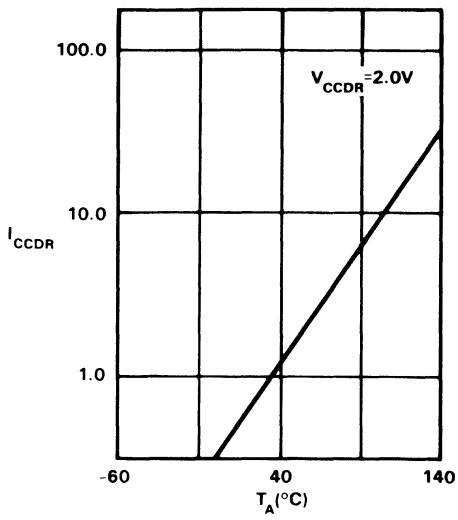
NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

I_{SB1} vs. V_{IN}



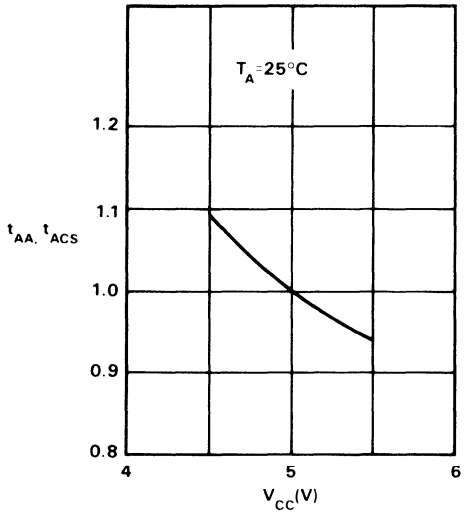
SRD6167-018

I_{CCDR} vs. Temperature



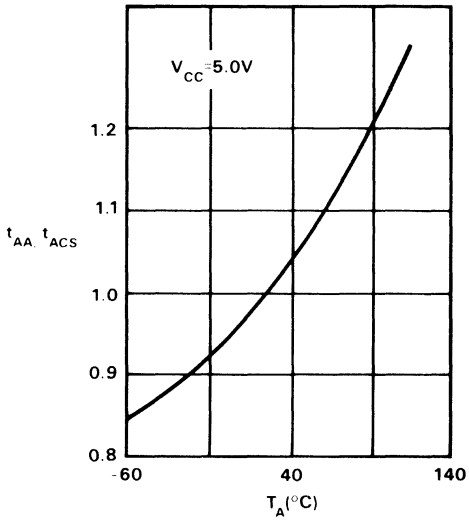
SRD6167-019

t_{AA}, t_{ACS} vs. Supply Voltage



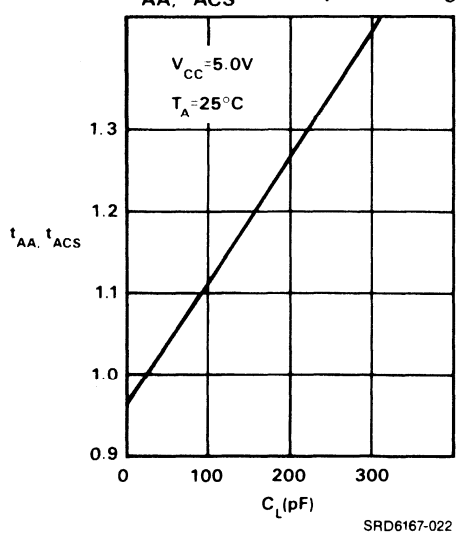
SRD6167-020

t_{AA}, t_{ACS} vs. Temperature



SRD6167-021

t_{AA}, t_{ACS} vs. Output Loading



SRD6167-022

CMOS STATIC RAMS 16K (4K × 4 BIT)

IDT6168SA
IDT6168LA

FEATURES:

- High-speed (equal access and cycle time)
  - —Military/Industrial - 35/45/55/70ns (max.)
  - —Commercial - 25/35/45/55ns (max.)
- Low power consumption
  - —IDT6168S
    - Active: 225mW (typ.)
    - Standby: 100μW (typ.)
  - —IDT6168L
    - Active: 225mW (typ.)
    - Standby: 10μW (typ.)
- Battery backup operation—2V data retention voltage (IDT6168L only)
- High-density 20-pin dual-in-line package and 20-pin leadless chip carriers
- Produced with advanced CEMOS™ high-performance technology
- CEMOS™ process virtually eliminates alpha particle soft-error rates (with no organic die coatings)
- Bidirectional data input and output
- Single 5V (± 10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Pin-compatible with standard 4K × 4 static RAMS
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT6168 is a 16,384-bit high-speed static RAM organized as 4K × 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS™. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

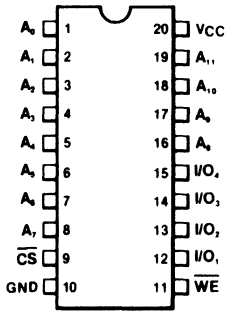
Access times as fast as 25ns are available with maximum power consumption of only 605mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consumes less than 100μW, typically. This capability provides significant system-level power and cooling savings. The low power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 1μW operating off of a 2V battery.

All inputs and outputs of the IDT6168 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT6168 is packaged in either a space-saving 20-pin, 300 mil DIP or 20-pin leadless chip carrier, providing high board-level packing densities.

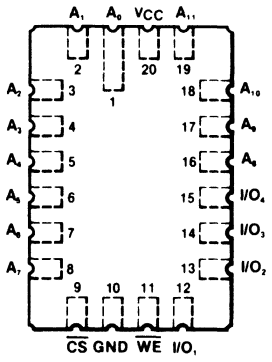
The IDT6168 Military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



SSD6168-001

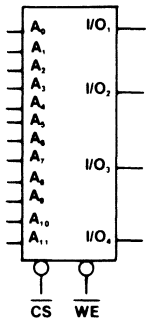
DIP
TOP VIEW



SSD6168-002

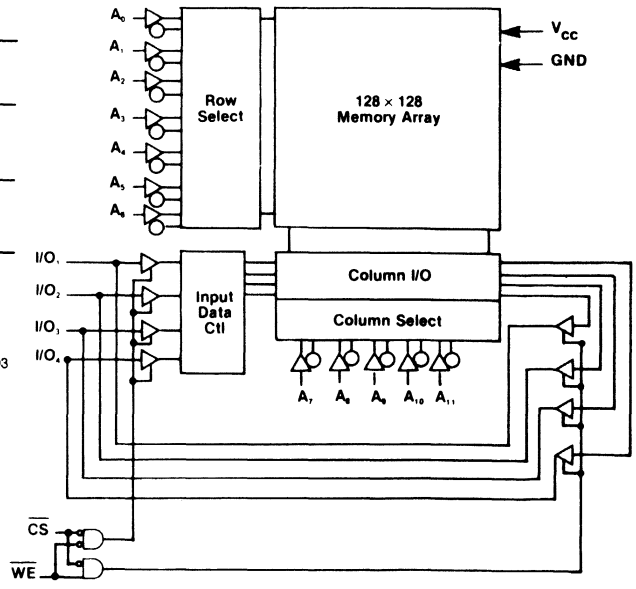
LCC
TOP VIEW

LOGIC SYMBOL



SSD6168-003

FUNCTIONAL BLOCK DIAGRAM



SSD6168-004

PIN NAMES

A_0-A_{11}	ADDRESS INPUTS	I/O_1-I/O_4	DATA INPUT/OUTPUT
$\overline{CS}$	CHIP SELECT	V_{CC}	POWER
$\overline{WE}$	WRITE ENABLE	GND	GROUND

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ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	°C
T_{STG}	Storage Temperature	−65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(1)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	−0.5 *	—	0.8	V

*V_{IL} min = −1.0V for pulse width less than 20ns.

NOTE:
1. Military (T_A = -55°C to +125°C)
Industrial (T_A = -40°C to +85°C)
Commercial (T_A = 0°C to +70°C)

DC ELECTRICAL CHARACTERISTICS V_{CC} = +5.0V ± 10%, $V_{CC(min.)}$ = 4.5V, $V_{CC(max.)}$ = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} −0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT6168SA MIN.	IDT6168SA TYP.(1)	IDT6168SA MAX.	IDT6168LA MIN.	IDT6168LA TYP.(1)	IDT6168LA MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			IND.	—	—	10	—	—	2	
			COM'L.	—	—	2	—	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			IND.	—	—	10	—	—	2	
			COM'L.	—	—	2	—	—	2	
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open V_{CC} = Max.	MIL.	—	45	110	—	45	90	mA
			IND.	—	45	110	—	45	90	
			COM'L.	—	45	110	—	45	90	
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100% V_{CC} = Max., Output Open	MIL.	—	45	110	—	45	90	mA
			IND.	—	45	110	—	45	90	
			COM'L.	—	45	110	—	45	90	
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$ V_{CC} = Max., Output Open Min. Duty Cycle = 100%	MIL.	—	5	35	—	5	25	mA
			IND.	—	5	35	—	5	25	
			COM'L.	—	5	35	—	5	25	
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{HC}$, V_{CC} = Max. $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	—	0.02	10	—	0.002	0.9	mA
			IND.	—	0.02	10	—	0.002	0.9	
			COM'L.	—	0.02	2	—	0.002	0.05	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		—	—	0.5	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

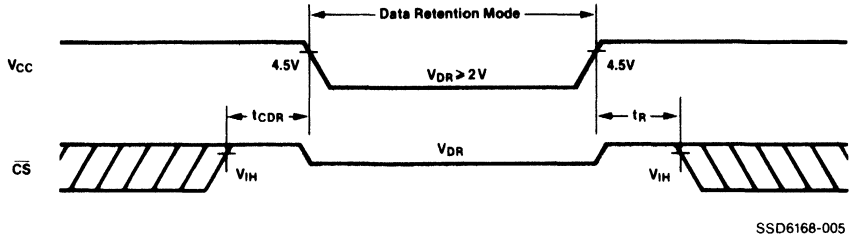
NOTE:
1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.

DATA RETENTION CHARACTERISTICS (T_A = -55°C to +125°C/-40°C to +85°C/0°C to +70°C) for L version only.

SYMBOL	PARAMETER	TEST CONDITIONS		IDT6168SA/LA MIN.	IDT6168SA/LA TYP.	IDT6168SA/LA MAX.	UNIT
V_{DR}	V_{CC} for Retention Data	$\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or ≤ 0.2V		2.0	—	—	V
I_{CCDR}	Data Retention Current		MIL.	—	0.5(2)	300(2)	µA
				—	1.0(3)	450(3)	
			IND.	—	0.5(2)	40(2)	µA
				—	1.0(3)	60(3)	
			COM'L.	—	0.5(2)	20(2)	µA
				—	1.0(3)	30(3)	
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R	Operation Recovery Time			t_{RC}(4)			ns

NOTES:
1. T_A = 25°C
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time

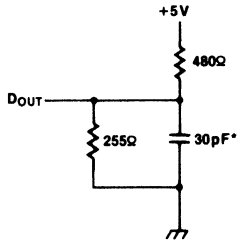
LOW V_{CC} DATA RETENTION WAVEFORM



SSD6168-005

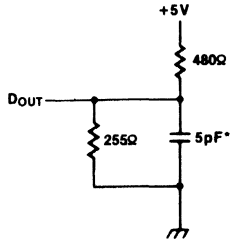
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2



SSD6168-006

Figure 1. Output Load



SSD6168-007

Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

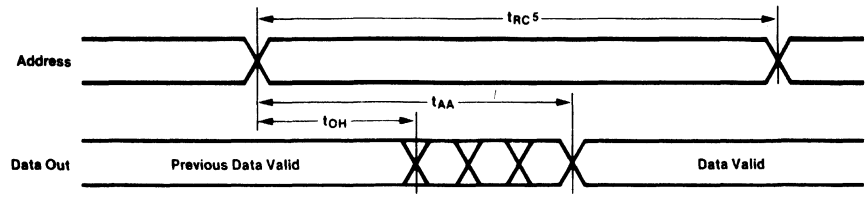
***Including scope and jig.**

AC CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT6168SA25(1) IDT6168LA25(1) MIN.	MAX.	IDT6168SA35 IDT6168LA35 MIN.	MAX.	IDT6168SA45 IDT6168LA45 MIN.	MAX.	IDT6168SA55 IDT6168LA55 MIN.	MAX.	IDT6168SA70(2) IDT6168LA70(2) MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	25	—	35	—	45	—	55	—	70	ns
t_{ACS}	Chip Select Access Time	—	25	—	35	—	45	—	55	—	70	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{LZ}(3)	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{HZ}(3)	Chip Deselection to Output in High Z	—	10	—	15	—	15	—	25	—	30	ns
t_{PU}(3)	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}(3)	Chip Selection to Power Down Time	—	25	—	35	—	40	—	50	—	60	ns
t_{RCS}	Read Command Set-Up Time	-5	—	-5	—	-5	—	-5	—	-5	—	ns
t_{RCH}	Read Command Hold Time	-5	—	-5	—	-5	—	-5	—	-5	—	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	20	—	30	—	40	—	50	—	60	—	ns
t_{CW}	Chip Selection to End of Write	20	—	30	—	40	—	50	—	60	—	ns
t_{AW}	Address Valid to End of Write	20	—	30	—	40	—	50	—	60	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	30	—	40	—	50	—	60	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	13	—	17	—	20	—	20	—	25	—	ns
t_{DH}	Data Hold Time	3	—	3	—	3	—	3	—	3	—	ns
t_{WZ}(3)	Write Enable to Output in High Z	—	7	—	13	—	20	—	25	—	30	ns
t_{OW}(3)	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

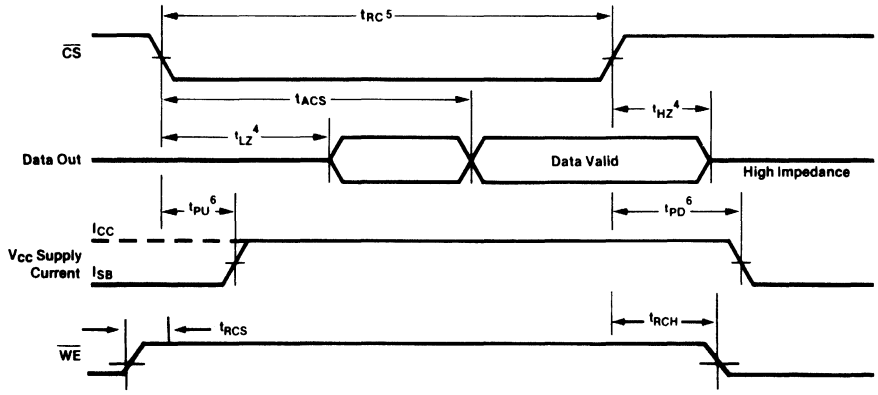
NOTES:
1. 0°C to +70°C only.
2. -40°C to +85°C and -55°C to +125°C only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1,2]



SSD6168-008

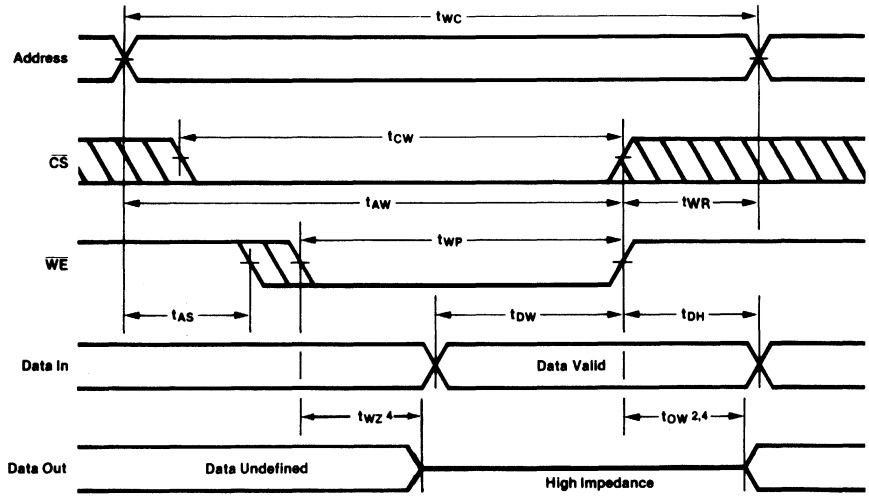
TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]



SSD6168-009

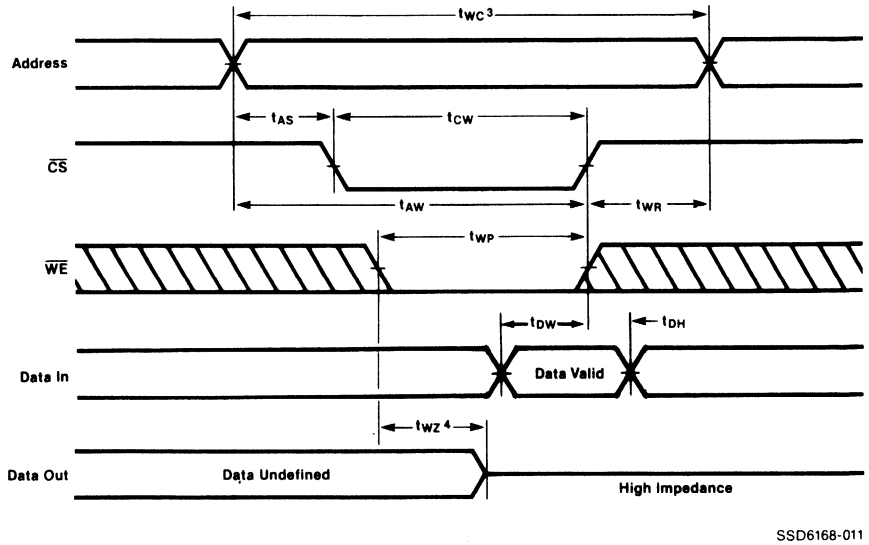
NOTES: 1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.
5. All READ cycle timings are referenced the last valid address to the first transitioning address.
6. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1]



SSD6168-010

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1]



NOTES: 1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

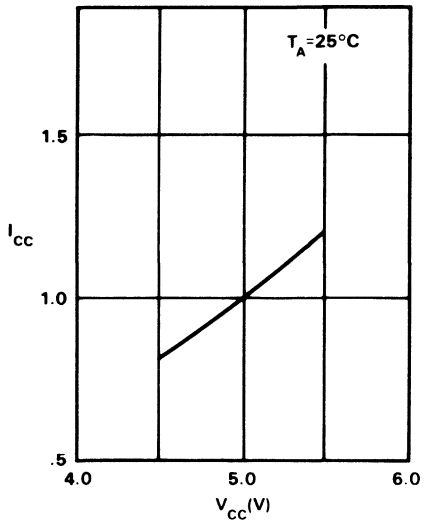
CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

SYMBOL	ITEM	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

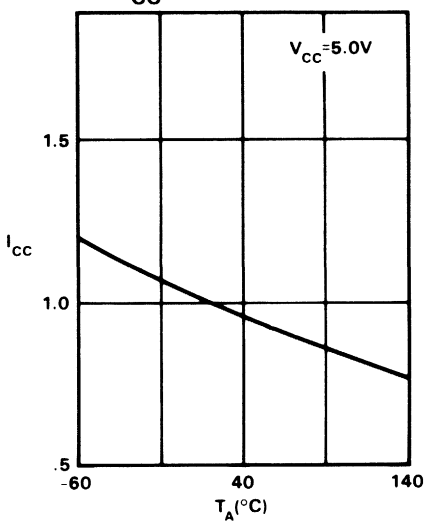
NOTE: This parameter is sampled and not 100% tested.

NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

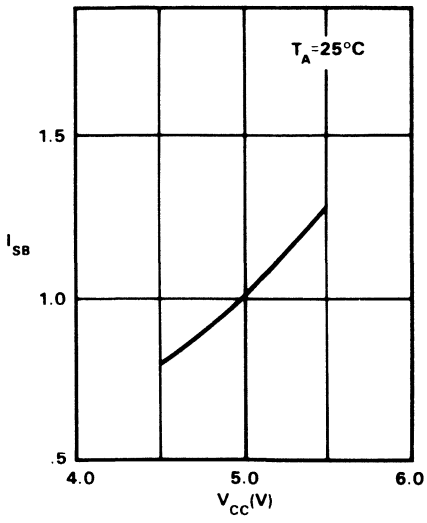
I_{CC} vs. Supply Voltage



I_{CC} vs. Temperature

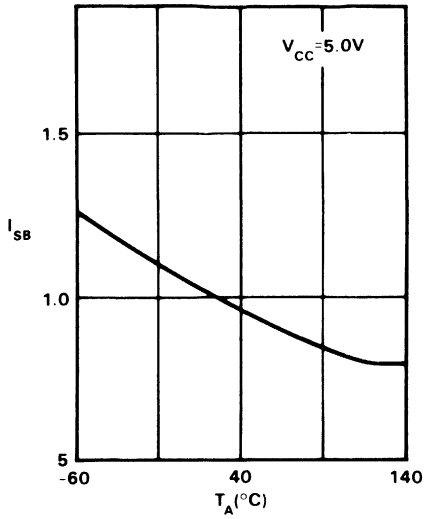


I_{SB} vs. Supply Voltage

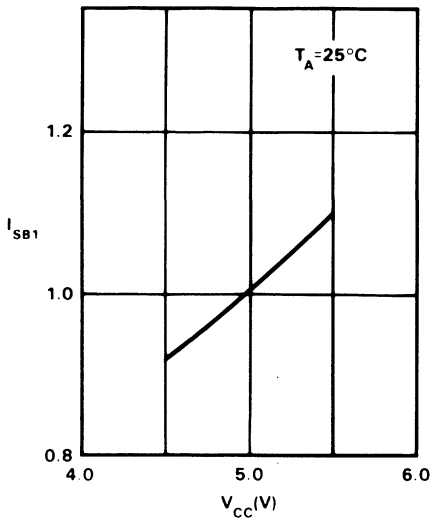


NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

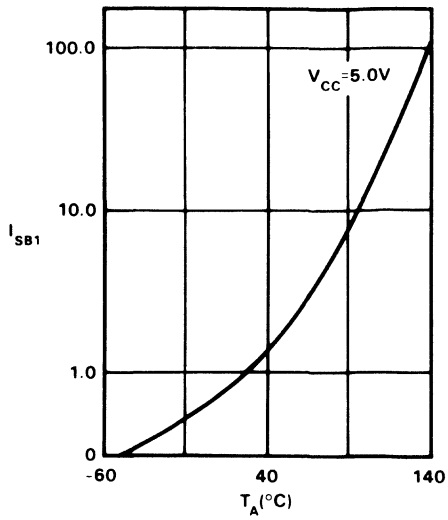
I_{SB} vs. Temperature



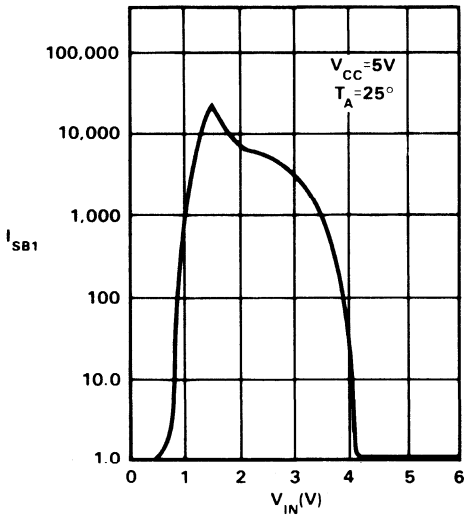
I_{SB1} vs. Supply Voltage



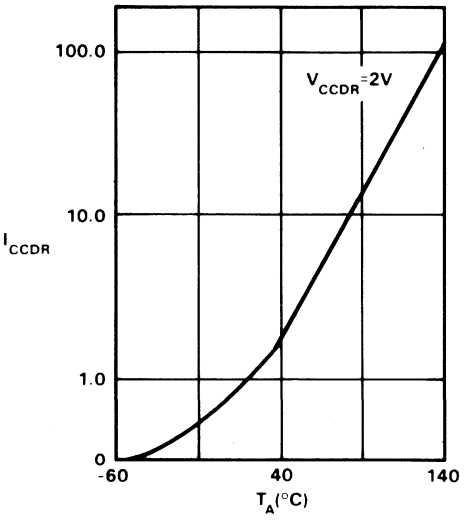
I_{SB1} vs. Temperature



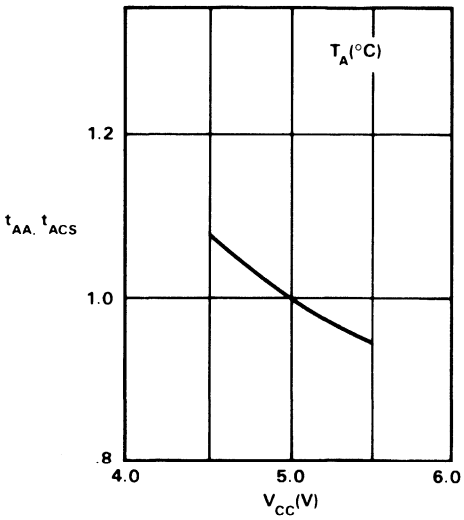
I_{SB1} vs. V_{IN}



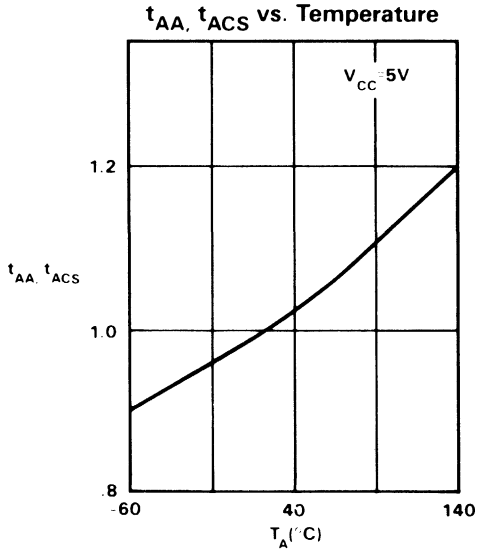
I_{CCDR} vs. Temperature



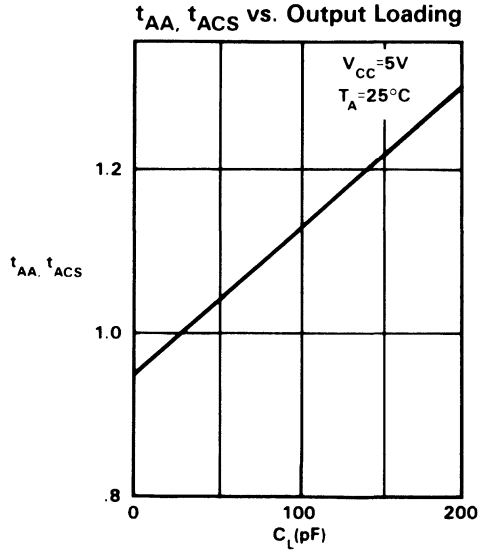
t_{AA}, t_{ACS} vs. Supply Voltage



t_{AA}, t_{ACS} vs. Temperature



t_{AA}, t_{ACS} vs. Output Loading



Integrated Device Technology, Inc.

CMOS STATIC RAMS 16K (4K × 4) BIT

IDT6168S
IDT6168L

FEATURES:

- High-speed (equal access and cycle time)
  - —Military/Industrial - 55/70/85/100ns (max.)
  - —Commercial - 45/55/70/85ns (max.)
- Low power consumption
  - —IDT6168S
    - Active: 225mW (typ.)
    - Standby: 100μW (typ.)
  - —IDT6168L
    - Active: 225mW (typ.)
    - Standby: 10μW (typ.)
- Battery backup operation—2V data retention voltage (IDT6168L only)
- High-density 20-pin dual-in-line package and 20-pin leadless chip carriers
- Produced with advanced CEMOS™ high-performance technology
- Bidirectional data input and output
- Single 5V (± 10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Pin-compatible with standard 4K × 4 static RAMS

DESCRIPTION:

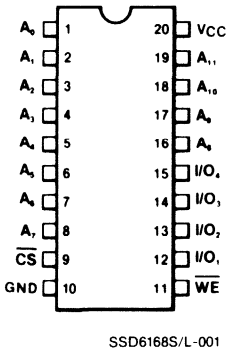
The IDT6168 is a 16,384-bit high-speed static RAM organized as 4K × 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS™. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

Access times as fast as 45ns are available with maximum power consumption of only 495mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consumes less than 100μW, typically. This capability provides significant system-level power and cooling savings. The low power, (L), version also offers a battery backup data retention capability where the circuit typically consumes only 1μW operating off of a 2V battery.

All inputs and outputs of the IDT6168 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

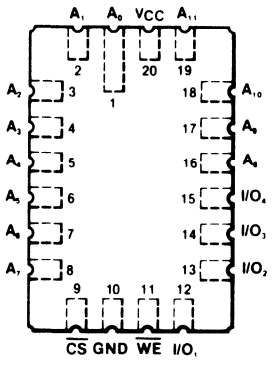
The IDT6168 is packaged in either a space-saving 20-pin, 300 mil DIP or 20-pin leadless chip carrier, providing high board-level packing densities.

PIN CONFIGURATIONS



SSD6168S/L-001

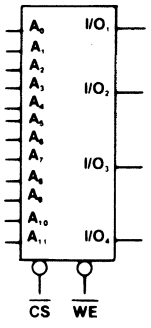
DIP
TOP VIEW



SSD6168S/L-002

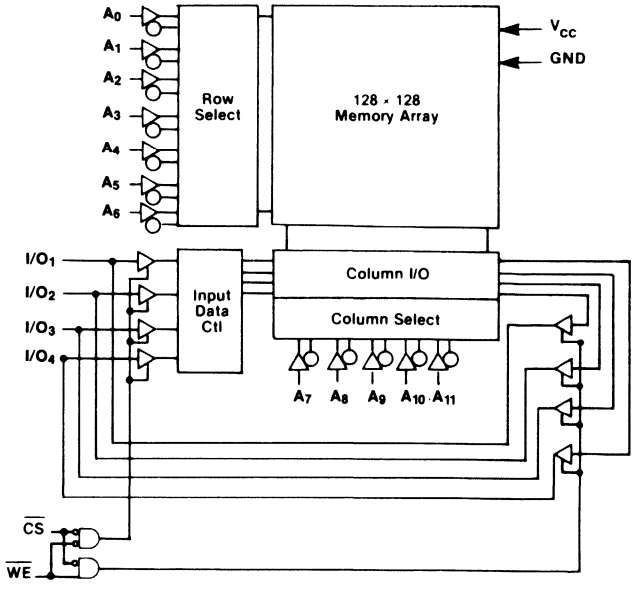
LCC
TOP VIEW

LOGIC SYMBOL



SSD6168S/L-003

FUNCTIONAL BLOCK DIAGRAM



SSD6168S/L-004

PIN NAMES

A_0-A_{11}	ADDRESS INPUTS	I/O_1-I/O_4	DATA INPUT/OUTPUT
$\overline{CS}$	CHIP SELECT	V_{CC}	POWER
$\overline{WE}$	WRITE ENABLE	GND	GROUND

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MILITARY, INDUSTRIAL, AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING		VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND		-0.5 to +7.0	V
T_A	Operating Temperature	COML. IND. MIL.	0 to +70 -40 to +85 -55 to +125	°C
T_{BIAS}	Temperature Under Bias		-65 to +135	°C
T_{STG}	Storage Temperature		-65 to +150	°C
P_T	Power Dissipation		1.0	W
I_{OUT}	DC Output Current		50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20 ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0V ± 10%, $V_{CC(min.)}$ = 4.5V, $V_{CC(max.)}$ = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V)

SYMBOL	PARAMETER	TEST CONDITIONS		IDT6168S MIN.	IDT6168S TYP.(1)	IDT6168S MAX.	IDT6168L MIN.	IDT6168L TYP.(1)	IDT6168L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL. IND. COM'L.	— — —	— — —	10 10 2	— — —	— — —	5 2 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. IND. COM'L.	— — —	— — —	10 10 2	— — —	— — —	5 2 2	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open V_{CC} = Max.	MIL. IND. COM'L.	— — —	45 45 45	90 90 90	— — —	45 45 45	90 90 90	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100% V_{CC} = Max., Output Open	MIL. IND. COM'L.	— — —	45 45 45	90 90 90	— — —	45 45 45	90 90 90	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} V_{CC} = Max., Output open Min. Duty Cycle = 100%	MIL. IND. COM'L.	— — —	5 5 5	20 20 20	— — —	5 5 5	20 20 20	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ ≥ V_{HC}, V_{CC} = Max. V_{IN} ≥ V_{HC} or ≤ V_{LC}	MIL. IND. COM'L.	— — —	0.02 0.02 0.02	10 2 2	— — —	0.002 0.002 0.002	0.9 0.150 0.050	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

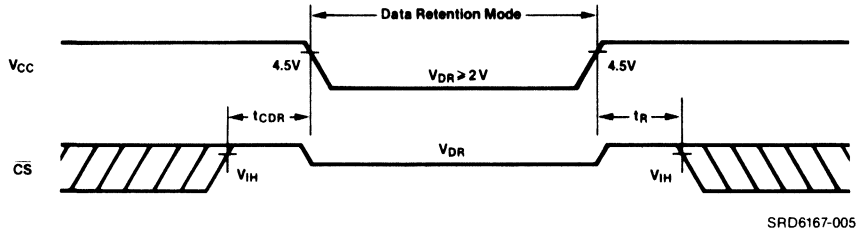
NOTE:
1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.

DATA RETENTION CHARACTERISTICS (T_A = -55°C to +125°C/-40°C to +85°C/0°C to +70°C) for L version only.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	IDT6168S/L TYP.	MAX.	UNIT
V_{DR}	V_{CC} for Retention Data	$\overline{CS}$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V		2.0	—	—	V
I_{CCDR}	Data Retention Current		MIL.	— —	0.5(2) 1.0(3)	300(2) 450(3)	µA
			IND.	— —	0.5(2) 1.0(3)	40(2) 60(3)	µA
			COM'L.	— —	0.5(2) 1.0(3)	20(2) 30(3)	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R	Operation Recovery Time			t_{RC}(4)			ns

NOTES:
1. T_A = 25°C
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM



SRD6167-005

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

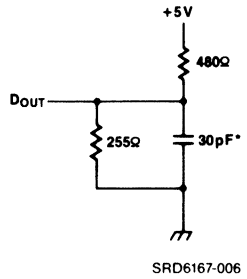


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Figure 1. Output Load

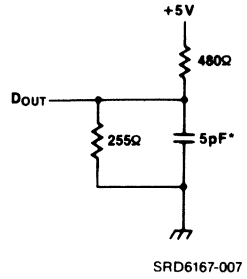

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Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

***Including scope and jig.**

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and -40°C to +85°C)

SYMBOL	PARAMETER	IDT6168S55 IDT6168L55 MIN.	MAX.	IDT6168S70 IDT6168L70 MIN.	MAX.	IDT6168S85 IDT6168L85 MIN.	MAX.	IDT6168S100 IDT6168L100 MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	55	—	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	70	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	55	—	70	—	85	—	100	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{LZ}(1)	Chip Selection to Output in Low Z	20	—	20	—	20	—	20	—	ns
t_{HZ}(1)	Chip Deselection to Output in High Z	—	25	—	30	—	40	—	50	ns
t_{PU}(1)	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Selection to Power Down Time	—	55	—	70	—	85	—	100	ns
t_{RCS}	Read Command Set-Up Time	-5	—	-5	—	-5	—	-5	—	ns
t_{RCH}	Read Command Hold Time	-5	—	-5	—	-5	—	-5	—	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	50	—	60	—	75	—	90	—	ns
t_{CW}	Chip Selection to End of Write	50	—	60	—	75	—	90	—	ns
t_{AW}	Address Valid to End of Write	50	—	60	—	75	—	90	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	50	—	60	—	75	—	90	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	25	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold Time	5	—	5	—	5	—	5	—	ns
t_{WZ}(1)	Write Enable to Output in High Z	—	25	—	30	—	40	—	50	ns
t_{OW}(1)	Output Active from End of Write	0	40	0	50	0	60	0	70	ns

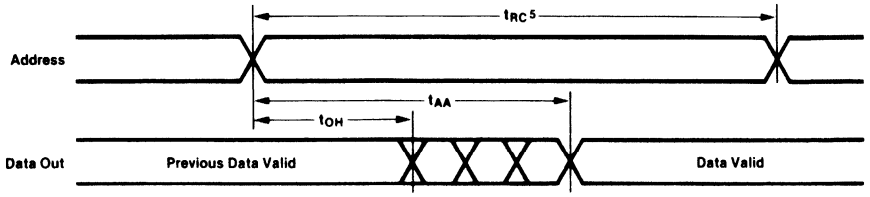
NOTE:
1. This parameter guaranteed but not tested.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT6168S45 IDT6168L45 MIN.	MAX.	IDT6168S55 IDT6168L55 MIN.	MAX.	IDT6168S70 IDT6168L70 MIN.	MAX.	IDT6168S85 IDT6168L85 MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	45	—	55	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	—	85	ns
t_{ACS}	Chip Select Access Time	—	45	—	55	—	70	—	85	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{LZ}(1)	Chip Selection to Output in Low Z	20	—	20	—	20	—	20	—	ns
t_{HZ}(1)	Chip Deselection to Output in High Z	—	20	—	25	—	25	—	25	ns
t_{PU}(1)	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Selection to Power Down Time	—	40	—	50	—	60	—	70	ns
t_{RCS}	Read Command Set-Up Time	-5	—	-5	—	-5	—	-5	—	ns
t_{RCH}	Read Command Hold Time	-5	—	-5	—	-5	—	-5	—	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	40	—	50	—	60	—	75	—	ns
t_{CW}	Chip Selection to End of Write	35	—	45	—	55	—	65	—	ns
t_{AW}	Address Valid to End of Write	35	—	45	—	55	—	65	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	35	—	45	—	55	—	70	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	15	—	20	—	25	—	30	—	ns
t_{DH}	Data Hold Time	3	—	3	—	3	—	3	—	ns
t_{WZ}(1)	Write Enable to Output in High Z	—	20	—	25	—	30	—	40	ns
t_{OW}(1)	Output Active from End of Write	10	40	10	50	10	60	10	70	ns

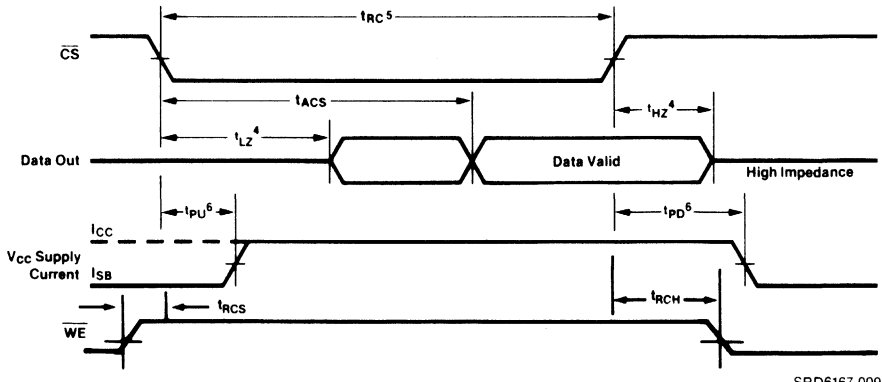
NOTE:
1. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1,2)



SRD6167-008

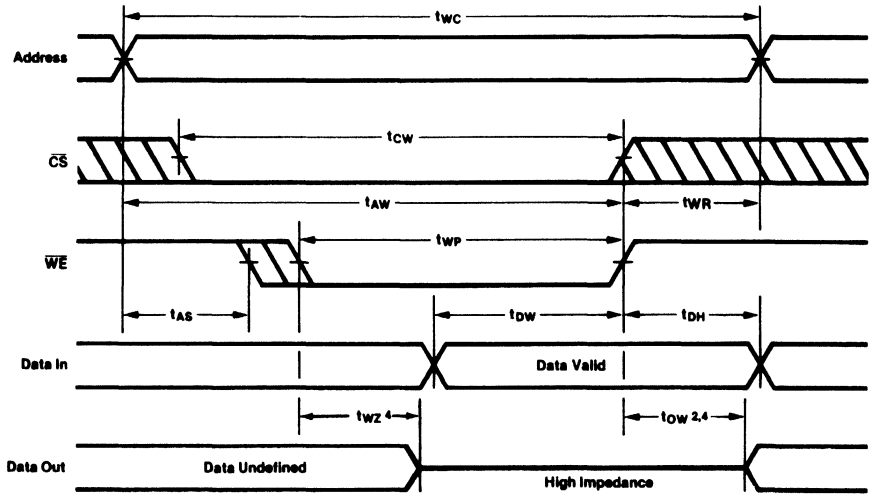
TIMING WAVEFORM OF READ CYCLE NO. 2(1,3)



SRD6167-009

NOTES: 1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter sampled but not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. This parameter is sampled but not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1]



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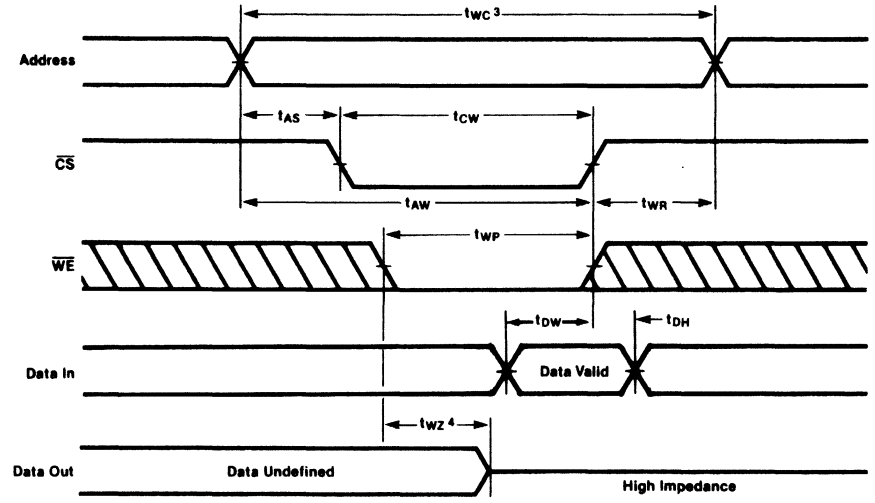
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1]



SRD6167-011

NOTES: 1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

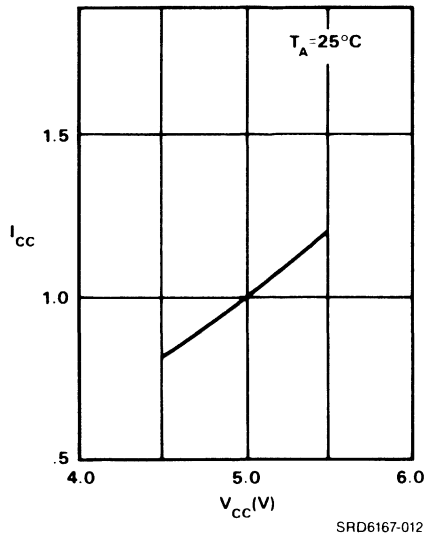
CAPACITANCE (T_A = +25°C, f = 1.0 MHz.)

SYMBOL	ITEM	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
This parameter is guaranteed but not tested.

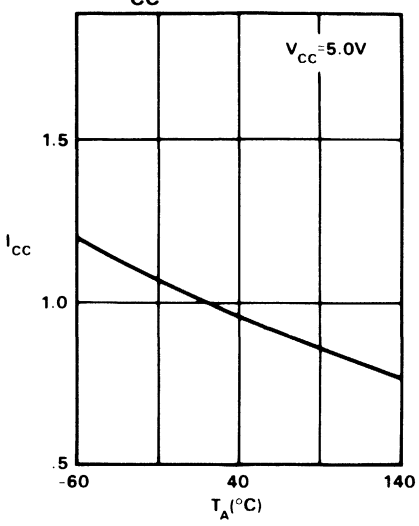
NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

I_{CC} vs. Supply Voltage



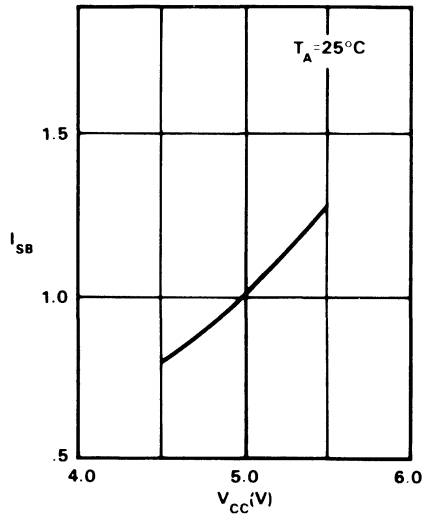
SRD6167-012

I_{CC} vs. Temperature



SRD6167-013

I_{SB} vs. Supply Voltage



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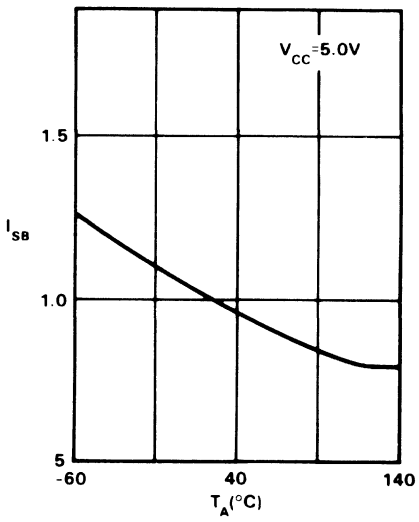
I_{SB} vs. Temperature



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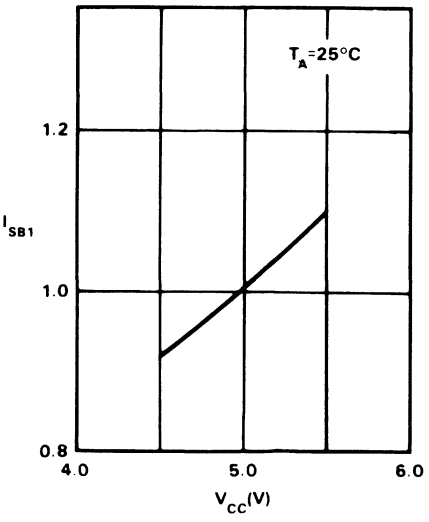
I_{SB1} vs. Supply Voltage



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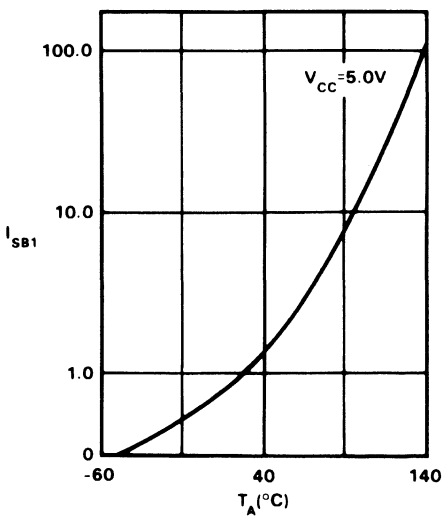
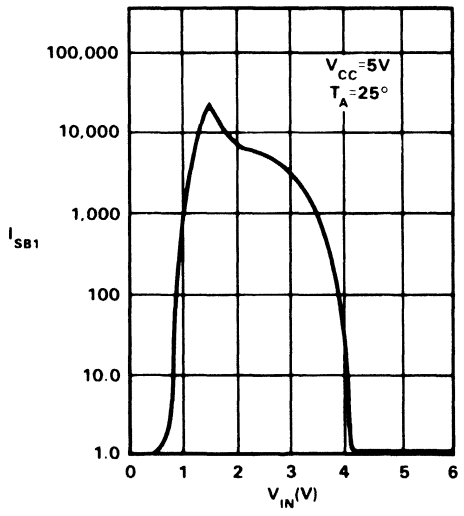
I_{SB1} vs. Temperature



SRD6167-017

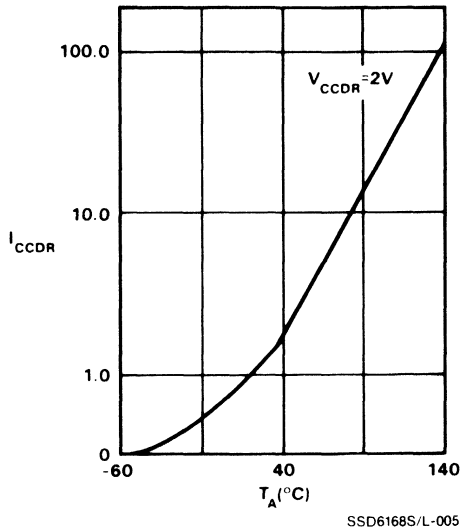
NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

I_{SB1} vs. V_{IN}



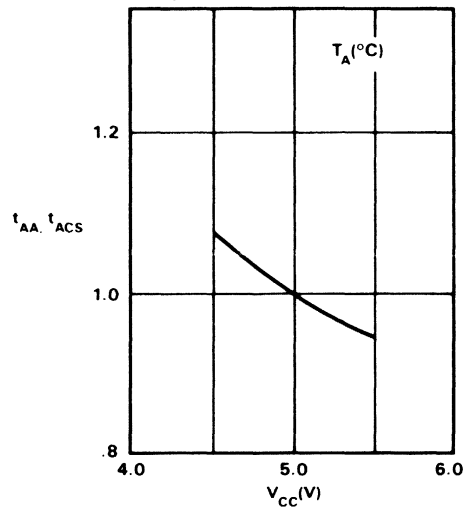
SRD6167-018

I_{CCDR} vs. Temperature



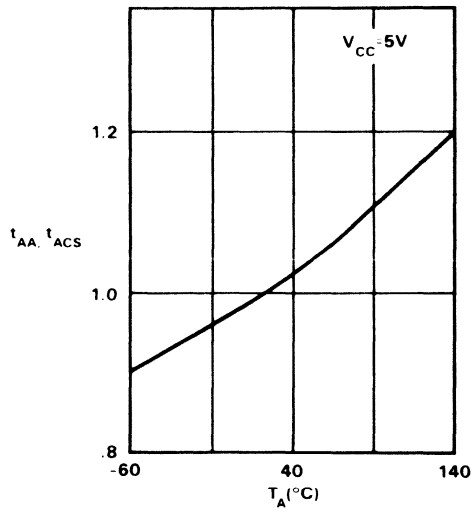
SSD6168S/L-005

t_{AA}, t_{ACS} vs. Supply Voltage



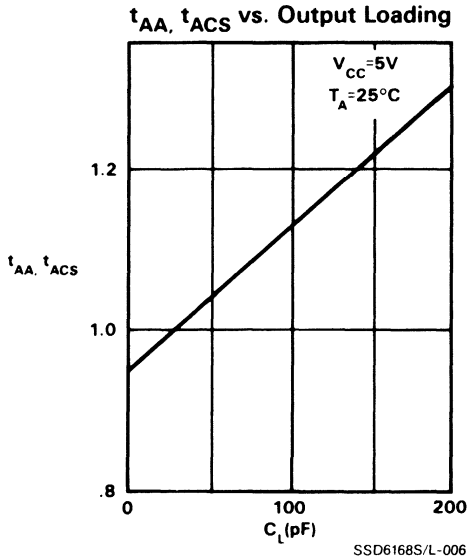
SRD6167-019

t_{AA}, t_{ACS} vs. Temperature



SSD6168S/L-007

t_{AA}, t_{ACS} vs. Output Loading



SSD6168S/L-006

Integrated Device Technology, Inc.

CMOS STATIC RAMS 16K (4K x 4 BIT)

SEPARATE DATA INPUTS AND OUTPUTS

IDT71681SA/LA
IDT71682SA/LA

FEATURES:

- Separate data inputs and outputs
- IDT71681S/L: outputs track inputs during write mode
- IDT71682S/L: high impedance outputs during write mode
- High-speed (equal access and cycle time)
  - —Military/Industrial — 35/45/55/70ns (max.)
  - —Commercial — 25/35/45/55ns (max.)
- Low power consumption
  - —IDT71681/2S
    Active: 225mW (Typ.)
    Standby: 100μW(Typ.)
  - —IDT71681/2L
    Active: 225mW (Typ.)
    Standby: 10μW(Typ.)
- Battery backup operation—2V data retention (L version only)
- High-density 24 pin 300-mil dual-in-line package and 28 pin leadless chip carriers
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates (with no organic die coatings)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT71681/IDT71682 are 16,384-bit high-speed static RAMs organized as 4K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

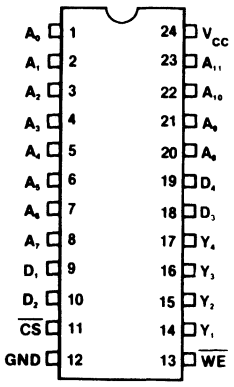
Access times as fast as 25ns are available with maximum power consumption of only 605mW. These circuits also offer a reduced power standby mode (I_{SB}). When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, this standby mode as long as $\overline{CS}$ remains high. In the ultra low power standby mode (I_{SB1}), the devices consume less than 10μW, typically. This capability provides significant system-level power and cooling savings. The low power (L) versions also offer a battery backup data retention capability where the circuit typically consumes only 1μW operating off a 2V battery.

All inputs and outputs of the IDT71681/IDT71682 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

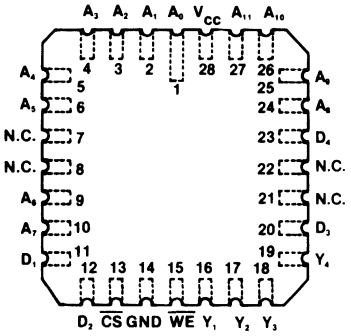
The IDT71681/IDT71682 are packaged in either space-saving 24-pin, 300 mil DIPs or 28-pin leadless chip carriers, providing high board-level packing densities.

The IDT71681/IDT71682 Military RAMs are 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS

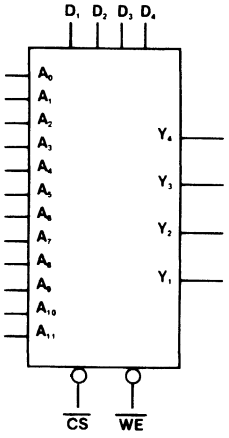


DIP
TOP VIEW

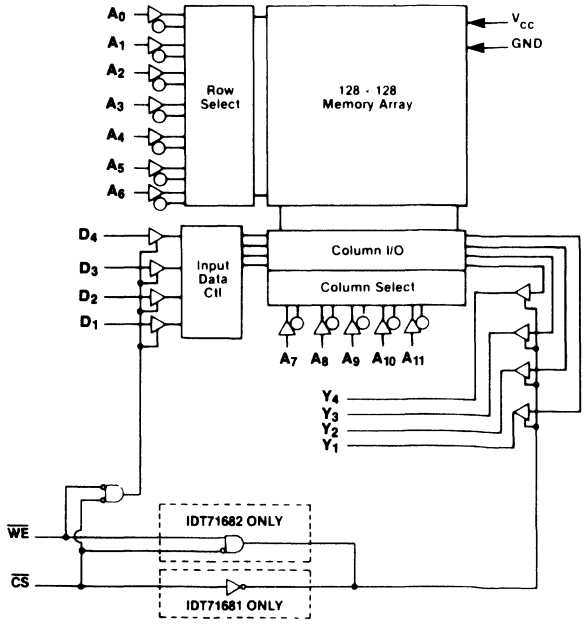


LCC
TOP VIEW

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0–A_{11}	ADDRESS INPUTS	D_1–D_4	DATA IN
$\overline{CS}$	CHIP SELECT	Y_1–Y_4	DATA OUT
$\overline{WE}$	WRITE ENABLE	GND	GROUND
V_{CC}	POWER		

CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY, INDUSTRIAL, AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
T_A	Operating Temperature	− 55 to + 125	°C
T_{BIAS}	Temperature Under Bias	− 65 to + 135	°C
T_{STG}	Storage Temperature	− 65 to + 150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20 ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS V_{CC} = +5.0V ± 10%, $V_{CC(min.)}$ = 4.5V, $V_{CC(max.)}$ = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} −0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71681/82SA MIN.	IDT71681/82SA TYP.[1]	IDT71681/82SA MAX.	IDT71681/82LA MIN.	IDT71681/82LA TYP.[1]	IDT71681/82LA MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			IND.	—	—	10	—	—	2	
			COM'L.	—	—	2	—	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			IND.	—	—	10	—	—	2	
			COM'L.	—	—	2	—	—	2	
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open V_{CC} = Max.	MIL.	—	45	110	—	45	90	mA
			IND.	—	45	110	—	45	90	
			COM'L.	—	45	110	—	45	90	
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100% V_{CC} = Max., Output Open	MIL.	—	45	110	—	45	90	mA
			IND.	—	45	110	—	45	90	
			COM'L.	—	45	110	—	45	90	
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$ V_{CC} = Max., Output Open Min. Duty Cycle = 100%	MIL.	—	5	35	—	5	25	mA
			IND.	—	5	35	—	5	25	
			COM'L.	—	5	35	—	5	25	
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{HC}$, V_{CC} = Max. $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	—	0.02	10	—	0.002	0.9	mA
			IND.	—	0.02	10	—	0.002	0.9	
			COM'L.	—	0.02	2	—	0.002	0.05	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		—	—	0.5	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

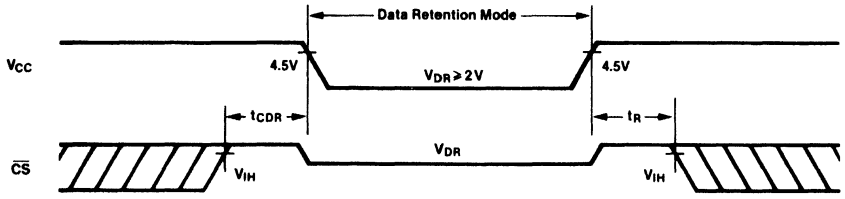
NOTES:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DATA RETENTION CHARACTERISTICS (T_A = -55°C to +125°C/-40°C to +85°C/0°C to +70°C) for L version only.

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71681SA/LA - IDT71682SA/LA MIN.	TYP.	MAX.	UNIT
V_{DR}	V_{CC} for Retention Data	$\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or ≤ 0.2V		2.0	—	—	V
I_{CCDR}	Data Retention Current		MIL.	— —	0.5(2) 1.0(3)	300(2) 450(3)	µA
			IND.	— —	0.5(2) 1.0(3)	40(2) 60(3)	µA
			COM'L.	— —	0.5(2) 1.0(3)	20(2) 30(3)	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R	Operation Recovery Time			t_{RC}(4)			ns

NOTES:
1. T_A = 25°C
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

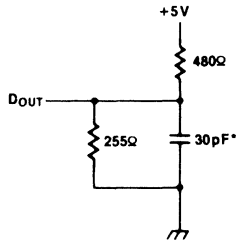


Figure 1. Output Load

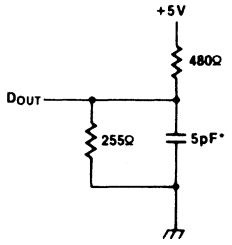


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

*Including scope and jig.

AC CHARACTERISTICS
(V_{CC} = 5V ± 10%, T_A = -55°C to =125°C/-40°C to +85°C/0°C to +70°C unless otherwise noted.)

SYMBOL	PARAMETER	IDT71681-25(1) IDT71682-25(1) MIN.	MAX.	IDT71681-35 IDT71682-35 MIN.	MAX.	IDT71681-45 IDT71682-45 MIN.	MAX.	IDT71681-55 IDT71682-55 MIN.	MAX.	IDT71681-70(2) IDT71682-70(2) MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	25	—	35	—	45	—	55	—	70	ns
t_{ACS}	Chip Select Access Time	—	25	—	35	—	45	—	55	—	70	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{LZ}(3)	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{HZ}(3)	Chip Deselection to Output in High Z	—	10	—	15	—	20	—	25	—	30	ns
t_{PU}(3)	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}(3)	Chip Selection to Power Down Time	—	25	—	35	—	40	—	50	—	60	ns
t_{RCS}	Read Command Set-Up Time	-5	—	-5	—	-5	—	-5	—	-5	—	ns
t_{RCH}	Read Command Hold Time	-5	—	-5	—	-5	—	-5	—	-5	—	ns

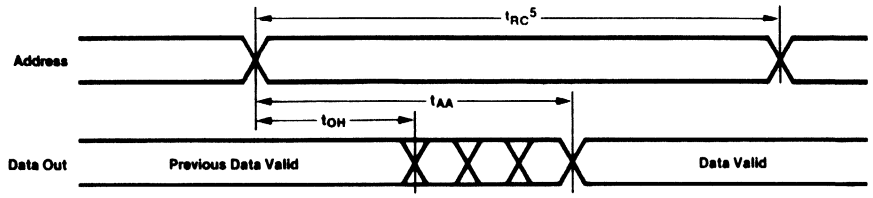
AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to =125°C/-40°C to +85°C/0°C to +70°C unless otherwise noted.)

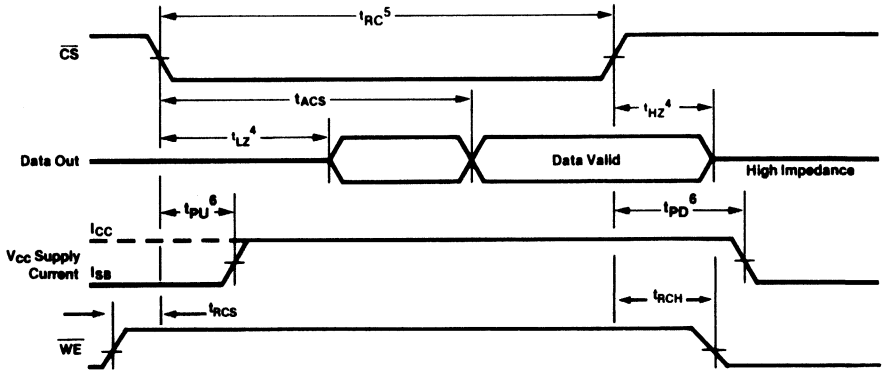
SYMBOL	PARAMETER	IDT71681-25[1] IDT71682-25[1] MIN.	MAX.	IDT71681-35 IDT71682-35 MIN.	MAX.	IDT71681-45 IDT71682-45 MIN.	MAX.	IDT71681-55 IDT71682-55 MIN.	MAX.	IDT71681-70[2] IDT71682-70[2] MIN.	MAX.	UNIT
WRITE CYCLE												
t_{WC}	Write Cycle Time	20	—	30	—	40	—	50	—	60	—	ns
t_{CW}	Chip Selection to End of Write	20	—	30	—	40	—	50	—	60	—	ns
t_{AW}	Address Valid to End of Write	20	—	30	—	40	—	50	—	60	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	13	—	17	—	20	—	20	—	25	—	ns
t_{DH}	Data Hold Time	3	—	3	—	3	—	3	—	3	—	ns
t_{IY}[3]	Data Valid to Output Valid (71681 only)	—	25	—	30	—	35	—	35	—	40	ns
t_{WY}[3]	Write Enable to Output Valid (71681 only)	—	25	—	30	—	35	—	35	—	40	ns
t_{WZ}[3]	Write Enable to Output in High Z (71682 only)	—	7	—	13	—	20	—	25	—	30	ns
t_{OW}[3]	Output Active from End of Write (71682 only)	0	—	0	—	0	—	0	—	0	—	ns

NOTES:
1. Available in Commercial 0°C to +70°C only.
2. Available in Military -55°C to +125°C and Industrial -40°C to +85°C only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1,2]

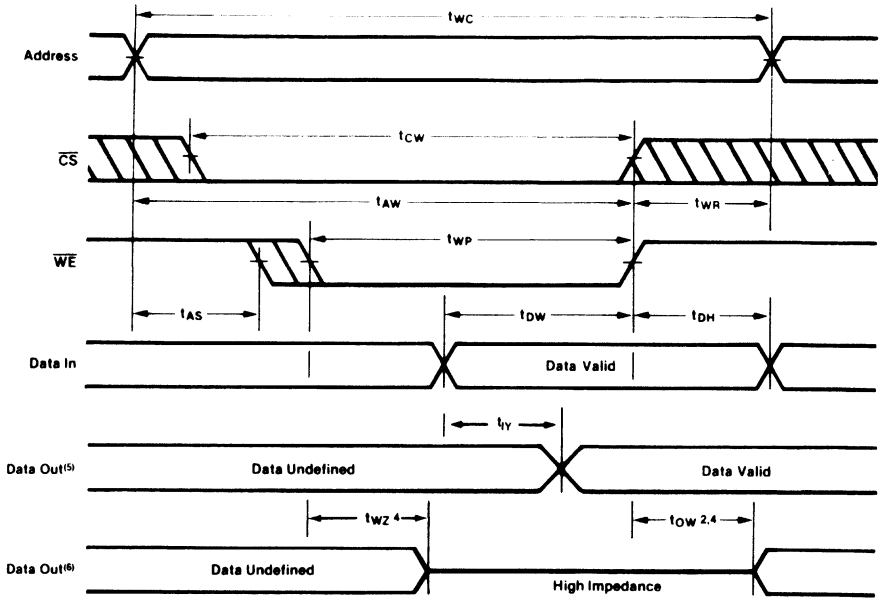


TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]

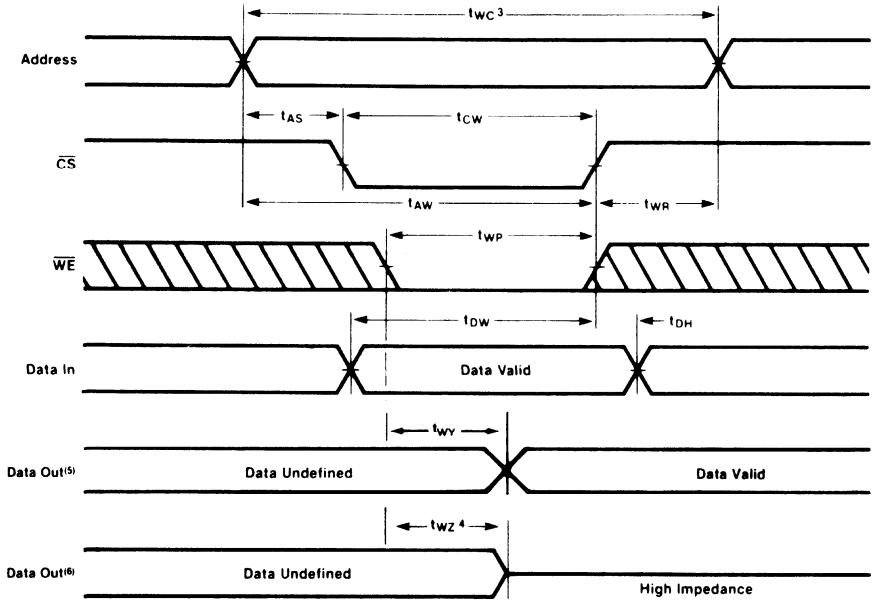


NOTES: 1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1]



NOTES: 1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.
5. For IDT71681 only.
6. For IDT71682 only.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write(1)	L	L	D_{IN}	Active
Write(2)	L	L	High Z	Active

NOTES:
1. For IDT71681 only.
2. For IDT71682 only.

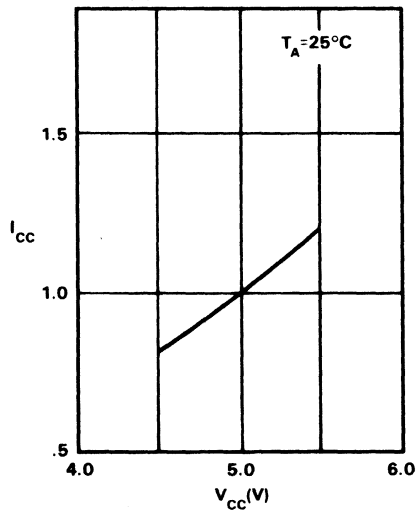
CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

SYMBOL	ITEM	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

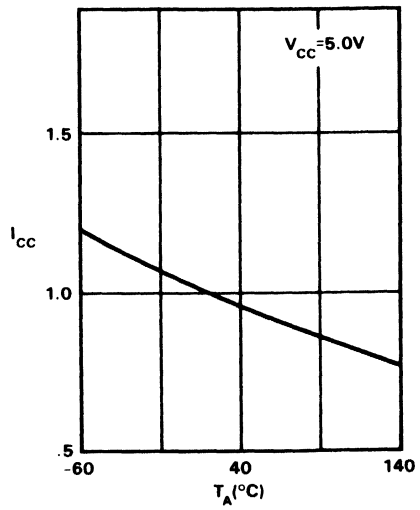
NOTE: This parameter is sampled and not 100% tested.

NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

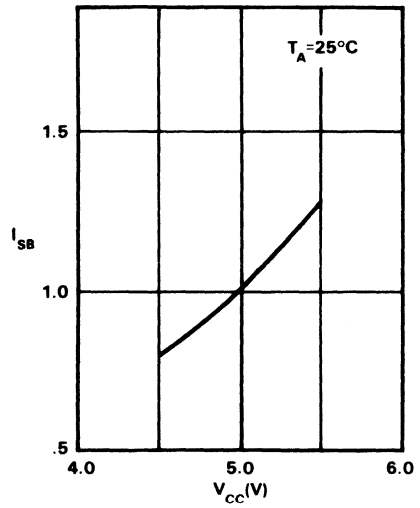
I_{CC} vs. Supply Voltage



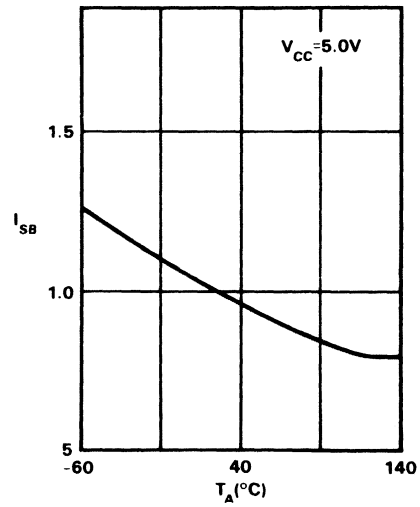
I_{CC} vs. Temperature



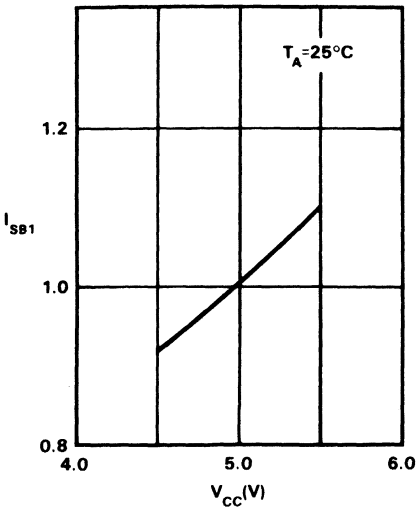
I_{SB} vs. Supply Voltage



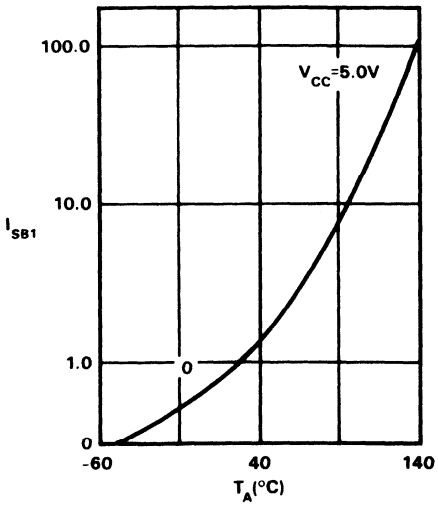
I_{SB} vs. Temperature



I_{SB1} vs. Supply Voltage

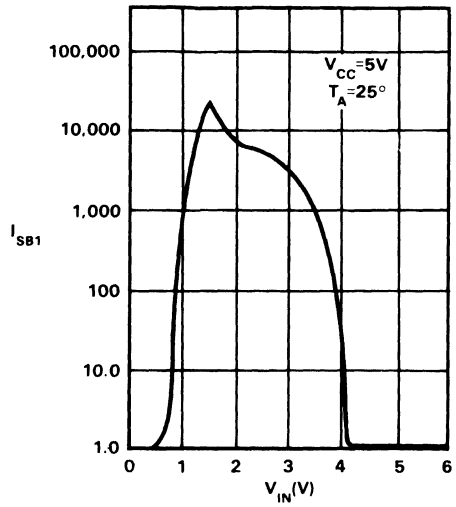


I_{SB1} vs. Temperature

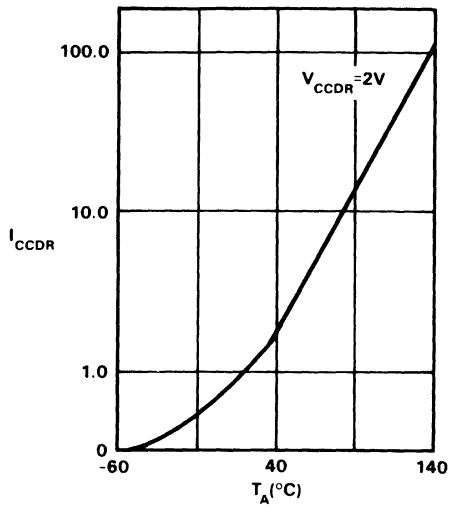


NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

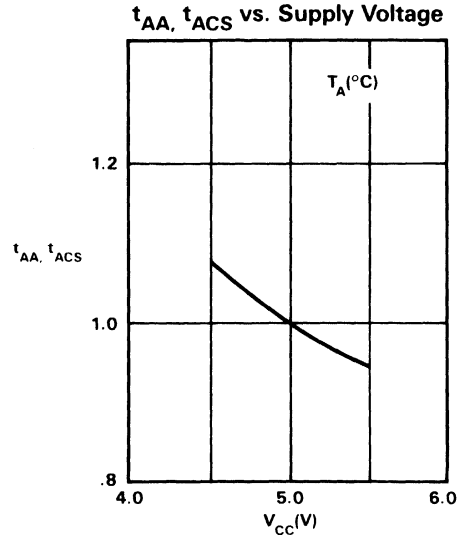
I_{SB1} vs. V_{IN}



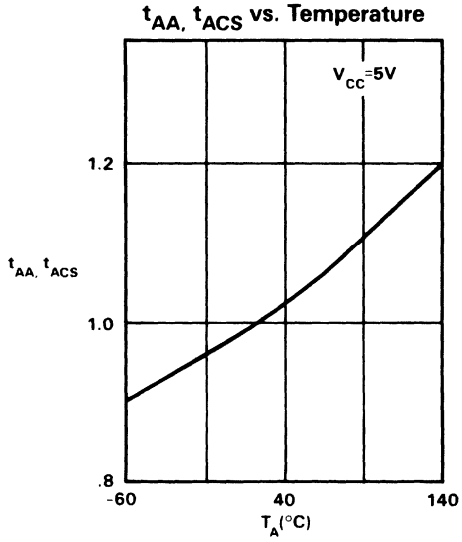
I_{CCDR} vs. Temperature



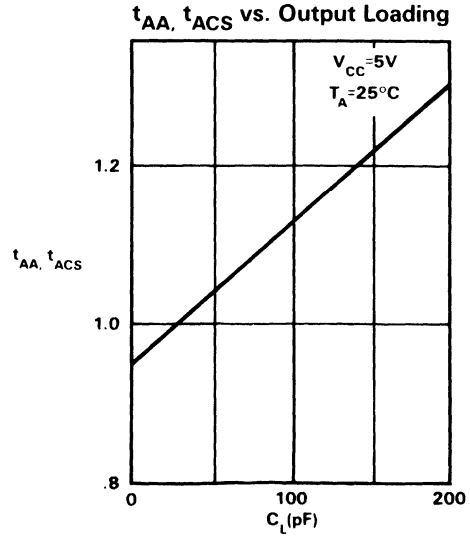
t_{AA}, t_{ACS} vs. Supply Voltage



t_{AA}, t_{ACS} vs. Temperature



t_{AA}, t_{ACS} vs. Output Loading



Integrated Device Technology Inc

CMOS STATIC RAMS 16K (4K × 4 BIT)

IDT71681S/L
IDT71682S/L

SEPARATE DATA INPUTS AND OUTPUTS

FEATURES:

- Separate data inputs and outputs
- High-speed (equal access and cycle time)
  - —Military/Industrial - 55/70/85/100ns (max.)
  - —Commercial - 45/55/70/85ns (max.)
- Low power consumption
  - —IDT71681S
    - Active: 225mW (typ.)
    - Standby: 100μW (typ.)
  - —IDT71681L
    - Active: 225mW (typ.)
    - Standby: 10μW (typ.)
- Battery backup operation—2V data retention voltage (IDT71681L only)
- High-density 24 pin 300-mil dual in-line package and 28 pin leadless chip carriers.
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Standard product 100% screened to MIL-STD-883 Class C
- Military product available 100% screened to Class B

DESCRIPTION:

The IDT71681 is a 16,384-bit high-speed static RAM organized as 4K×4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS™. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

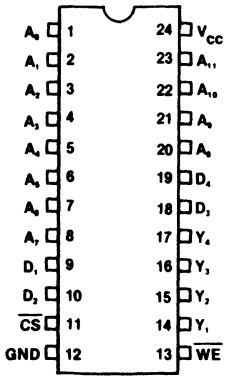
Access times as fast as 45ns are available with maximum power consumption of only 495mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consume less than 10μW, typically. This capability provides significant system-level power and cooling savings. The low power, (L), version also offers a battery backup data retention capability where the circuit typically consumes only 1μW operating off of a 2V battery.

All inputs and outputs of the IDT71681 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

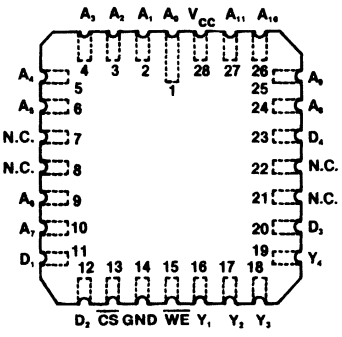
The IDT71681 is packaged in a space-saving 24-pin, 300 mil DIP or a 28-pin leadless chip carrier, providing high board-level packing densities.

The IDT71681 Military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS

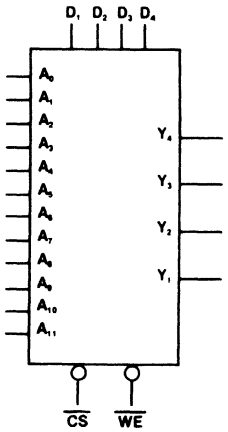


DIP
TOP VIEW

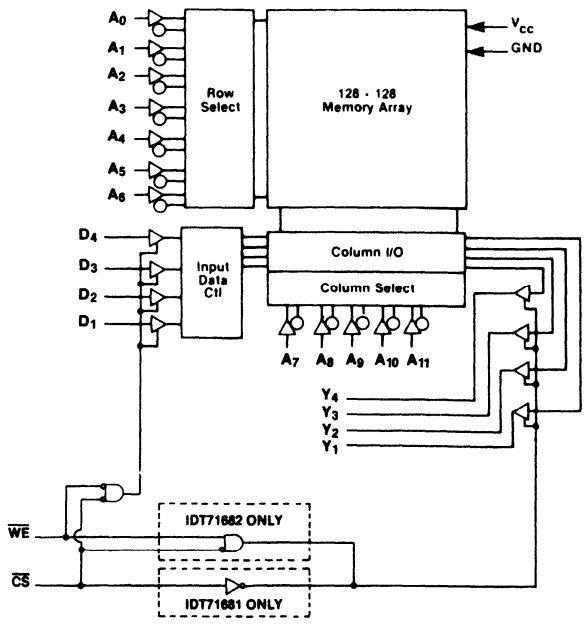


LCC
TOP VIEW

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0–A_{11}	ADDRESS INPUTS	D_1–D_4	DATA IN
$\overline{CS}$	CHIP SELECT	Y_1–Y_4	DATA OUT
$\overline{WE}$	WRITE ENABLE	GND	GROUND
V_{CC}	POWER		

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Printed in U.S.A.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
T_A	Operating Temperature	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−65 to +135	°C
T_{STG}	Storage Temperature	−65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
1. V_{IL} = -3.0V for pulse width less than 30 ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0V ± 10%, $V_{CC(min.)}$ = 4.5V, $V_{CC(max.)}$ = 5.5V, V_{LC} = 0.2V, V_{LC} = V_{CC} - 0.2V)

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71681/82S MIN.	IDT71681/82S TYP.[1]	IDT71681/82S MAX.	IDT71681/82L MIN.	IDT71681/82L TYP.[1]	IDT71681/82L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			IND.	—	—	10	—	—	2	
			COM'L.	—	—	2	—	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			IND.	—	—	10	—	—	2	
			COM'L.	—	—	2	—	—	2	
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open V_{CC} = Max.	MIL.	—	45	90	—	45	90	mA
			IND.	—	45	90	—	45	90	
			COM'L.	—	45	90	—	45	90	
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100% V_{CC} = Max., Output Open	MIL.	—	45	90	—	45	90	mA
			IND.	—	45	90	—	45	90	
			COM'L.	—	45	90	—	45	90	
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$ V_{CC} = Max., Output Open Min. Duty Cycle = 100%	MIL.	—	5	20	—	5	20	mA
			IND.	—	5	20	—	5	20	
			COM'L.	—	5	20	—	5	20	
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{HC}$, V_{CC} = Max. $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	—	0.02	10	—	0.002	0.9	mA
			IND.	—	0.02	2	—	0.002	0.150	
			COM'L.	—	0.02	2	—	0.002	0.050	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

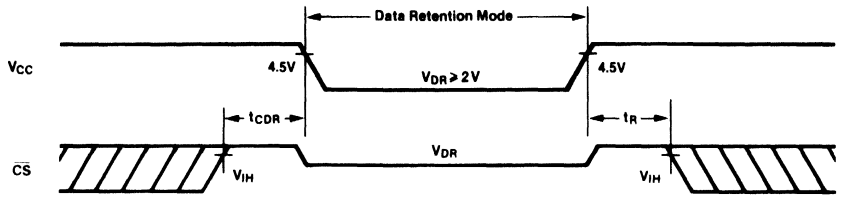
NOTE:
1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.

DATA RETENTION CHARACTERISTICS (T_A = -55°C to +125°C/-40°C to +85°C/0°C to +70°C) for L version only.

SYMBOL	PARAMETER	TEST CONDITIONS		IDT761681S/IDT761681L MIN.	IDT761681S/IDT761681L TYP.	IDT761681S/IDT761681L MAX.	UNIT
V_{DR}	V_{CC} for Retention Data	$\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or ≤ 0.2V		2.0	—	—	V
I_{CCDR}	Data Retention Current		MIL.	—	0.5[2]	300[2]	µA
				—	1.0[3]	450[3]	
			IND.	—	0.5[2]	40[2]	µA
				—	1.0[3]	60[3]	
			COM'L.	—	0.5[2]	20[2]	µA
				—	1.0[3]	30[3]	
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R	Operation Recovery Time			t_{RC}[4]			ns

NOTES:
1. T_A = 25°C
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

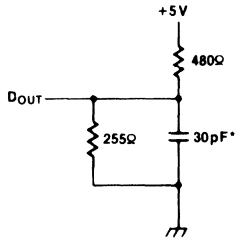


Figure 1. Output Load

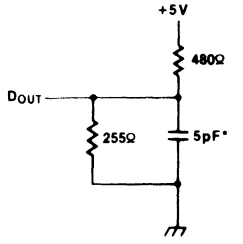


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and -40°C to +85°C)

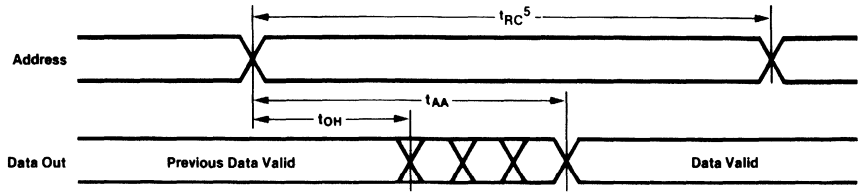
SYMBOL	PARAMETER	IDT71681/82S55 IDT71681/82L55 MIN.	MAX.	IDT71681/82S70 IDT71681/82L70 MIN.	MAX.	IDT71681/82S85 IDT71681/82L85 MIN.	MAX.	IDT71681/82S100 IDT71681/82L100 MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	55	—	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	70	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	55	—	70	—	85	—	100	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{LZ}(3)	Chip Selection to Output in Low Z	20	—	20	—	20	—	20	—	ns
t_{HZ}(3)	Chip Deselection to Output in High Z	—	25	—	30	—	40	—	50	ns
t_{PU}(3)	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(3)	Chip Selection to Power Down Time	—	55	—	70	—	85	—	100	ns
t_{RCS}	Read Command Set-Up Time	-5	—	-5	—	-5	—	-5	—	ns
t_{RCH}	Read Command Hold Time	-5	—	-5	—	-5	—	-5	—	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	45	—	55	—	65	—	80	—	ns
t_{CW}	Chip Selection to End of Write	45	—	55	—	65	—	80	—	ns
t_{AW}	Address Valid to End of Write	45	—	55	—	65	—	80	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	35	—	40	—	45	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	25	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold Time	5	—	5	—	5	—	5	—	ns
t_{IY}(3)	Data Valid to Output Valid(1)	—	35	—	40	—	45	—	50	ns
t_{WY}(3)	Write Enable to Output in Valid(1)	—	35	—	40	—	45	—	50	ns
t_{WZ}(3)	Write Enable to Output in High Z(2)	—	25	—	30	—	40	—	50	ns
t_{OW}(3)	Output Active from End of Write(2)	0	40	0	50	0	60	0	70	ns

AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0 to +70°C)

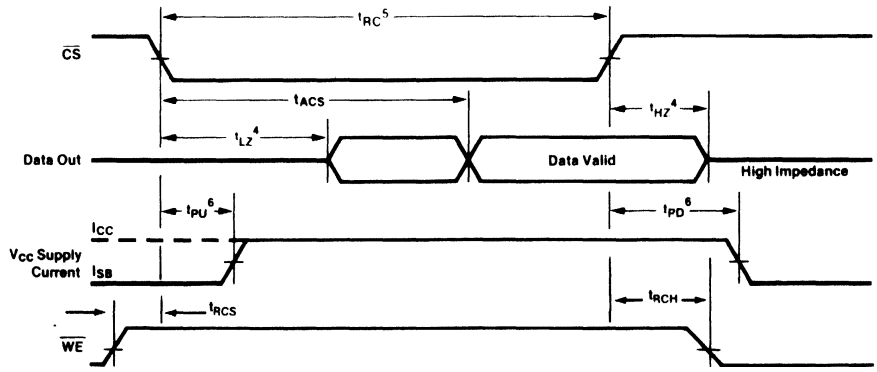
SYMBOL	PARAMETER	IDT71681/82S45 IDT71681/82L45 MIN.	MAX.	IDT71681/82S55 IDT71681/82L55 MIN.	MAX.	IDT71681/82S70 IDT71681/82L70 MIN.	MAX.	IDT71681/82S80 IDT71681/82L85 MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	45	—	55	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	—	85	ns
t_{ACS}	Chip Select Access Time	—	45	—	55	—	70	—	85	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{LZ}(3)	Chip Selection to Output in Low Z	20	—	20	—	20	—	20	—	ns
t_{HZ}(3)	Chip Deselection to Output in High Z	—	20	—	25	—	30	—	40	ns
t_{PU}(3)	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(3)	Chip Selection to Power Down Time	—	40	—	50	—	60	—	70	ns
t_{RCS}	Read Command Set-Up Time	-5	—	-5	—	-5	—	-5	—	ns
t_{RCH}	Read Command Hold Time	-5	—	-5	—	-5	—	-5	—	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	40	—	50	—	60	—	70	—	ns
t_{CW}	Chip Selection to End of Write	35	—	45	—	55	—	66	—	ns
t_{AW}	Address Valid to End of Write	35	—	45	—	55	—	65	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	30	—	35	—	40	—	45	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	15	—	20	—	25	—	30	—	ns
t_{DH}	Data Hold Time	3	—	3	—	3	—	3	—	ns
t_{IY}	Data Valid to Output Valid(1)	—	35	—	40	—	45	—	50	ns
t_{WY}	Write Enable to Output in Valid(1)	—	35	—	40	—	45	—	50	ns
t_{WZ}(3)	Write Enable to Output in High Z(2)	—	20	—	25	—	30	—	40	ns
t_{OW}(3)	Output Active from End of Write(2)	0	40	0	50	0	60	0	70	ns

NOTES:
1. For IDT71681 only.
2. For IDT71682 only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1,2)

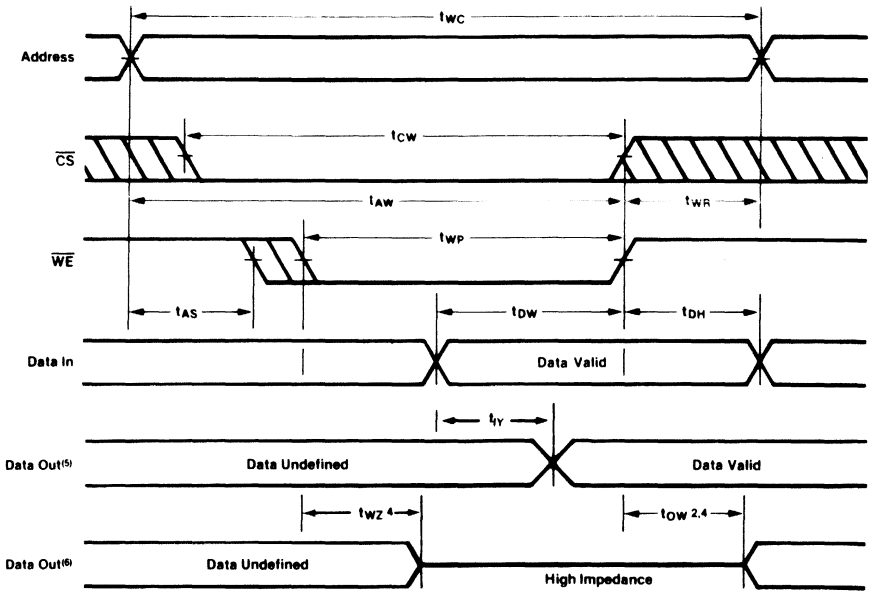


TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]

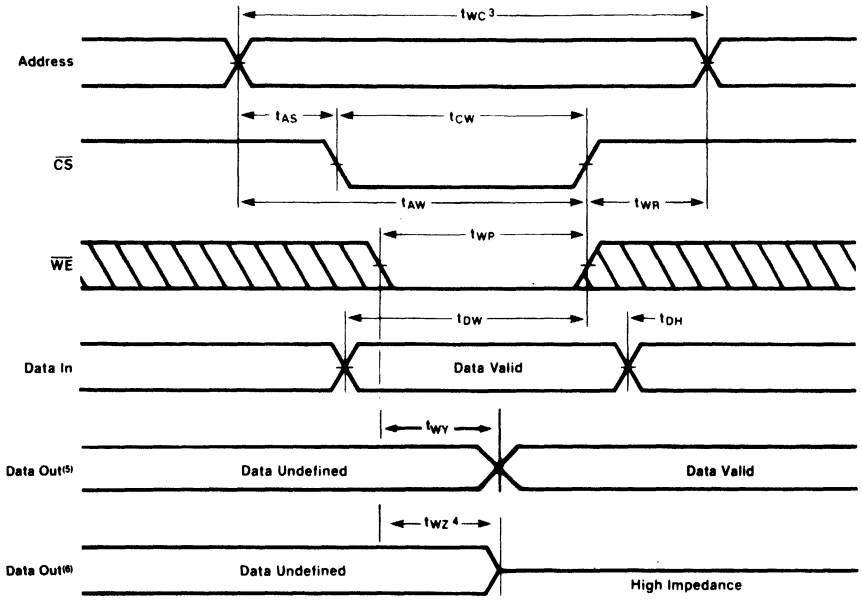


NOTES: 1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.
5. All READ cycle timings are referenced the last valid address to the first transitioning address.
6. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1]



NOTES: 1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.
5. For IDT71681 only.
6. For IDT71682 only.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write(1)	L	L	D_{IN}	Active
Write(2)	L	L	High Z	Active

NOTES:
1. For IDT71681 only.
2. For IDT71682 only.

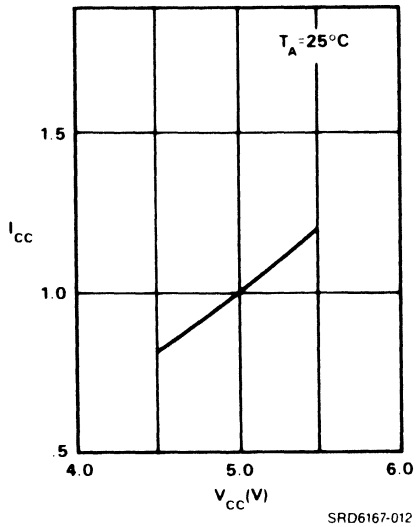
CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

SYMBOL	ITEM	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: This parameter is sampled and not 100% tested.

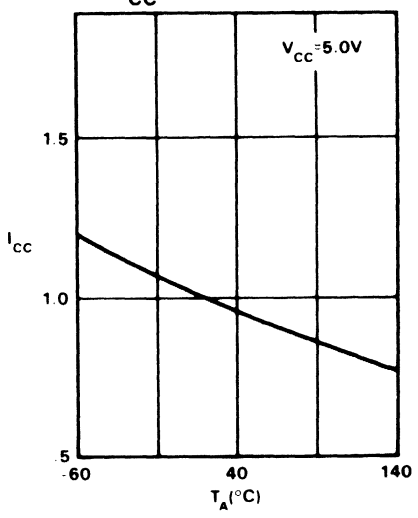
NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

I_{CC} vs. Supply Voltage



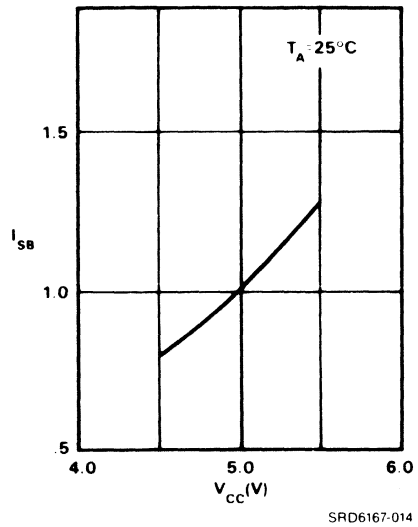
SRD6167-012

I_{CC} vs. Temperature



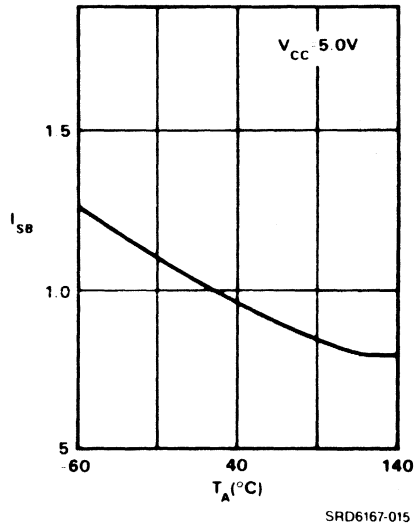
SRD6167-013

I_{SB} vs. Supply Voltage



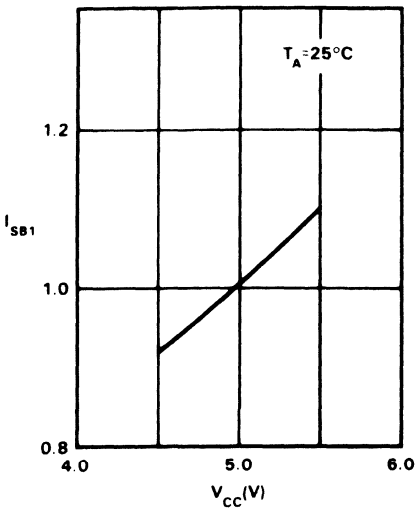
SRD6167-014

I_{SB} vs. Temperature



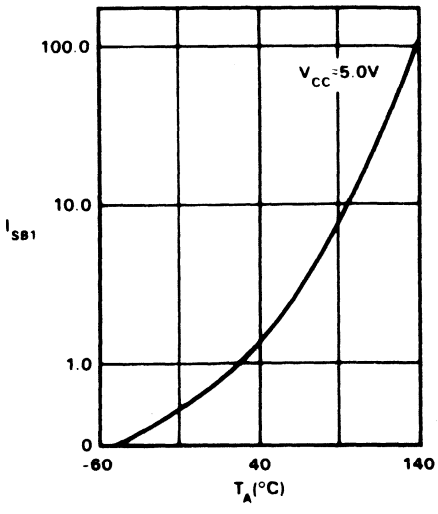
SRD6167-015

I_{SB1} vs. Supply Voltage



SRD6167-016

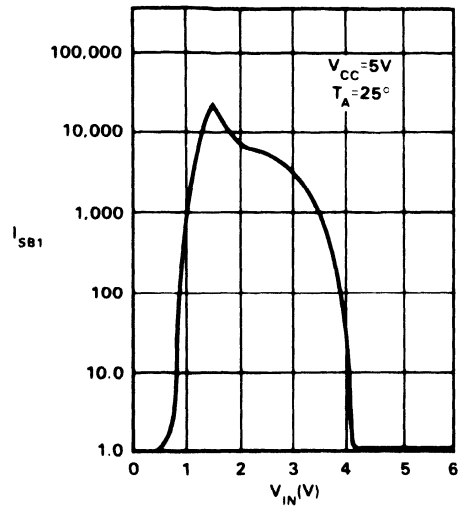
I_{SB1} vs. Temperature



SRD6167-017

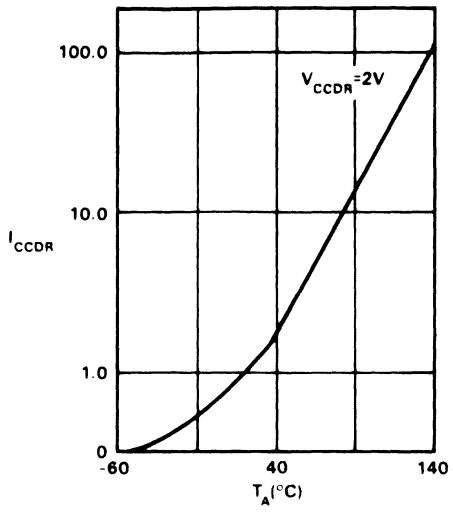
NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

I_{SB1} vs. V_{IN}



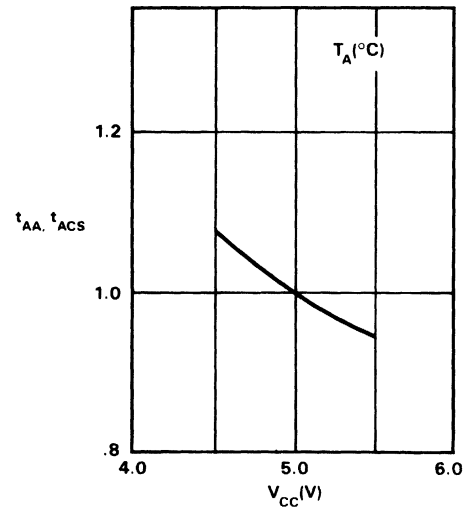
SRD6167-018

I_{CCDR} vs. Temperature



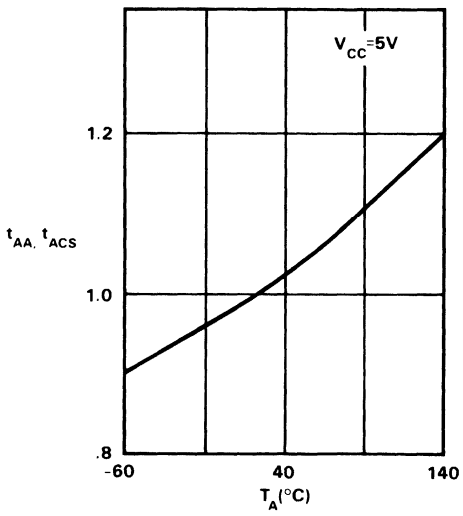
SSD6168S/L-005

t_{AA}, t_{ACS} vs. Supply Voltage



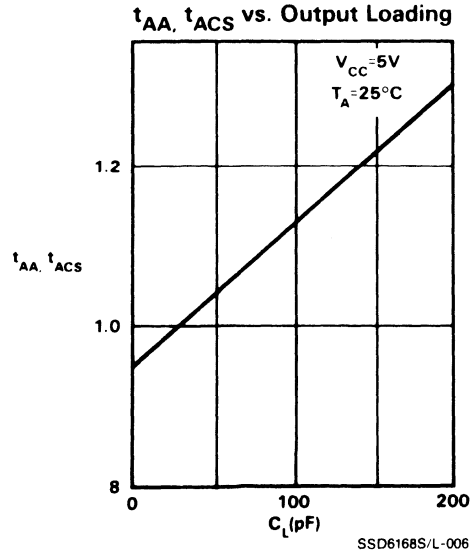
SRD6167-019

t_{AA}, t_{ACS} vs. Temperature



SSD6168S/L-007

t_{AA}, t_{ACS} vs. Output Loading



SSD6168S/L-006

Integrated Device Technology, Inc

CMOS STATIC RAMS 16K (2K x 8 BIT)

IDT6116S
IDT6116L

FEATURES:

- High-speed address/chip select access time
  - Military and Industrial
    - 55/50, 70/65,90/90, 120/120, 150/150 ns (max.)
  - Commercial
    - 55/50, 70/70, 90/90, 120/120, 150/150 ns (max.)
- Low-power operation
  - —IDT6116S
    - Active: 180mW (typ.)
    - Standby: 100μW (typ.)
  - —IDT6116L
    - Active: 160mW (typ.)
    - Standby: 20μW (typ.)
- Battery backup operation — 2V data retention voltage
- Produced with advanced CEMOS™ II high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Standard 24-pin DIP, 24-pin THINDIP, 28-pin and 32-pin LCC, or 24-Lead Flatpack
- Pin compatible with standard 16K static RAM and EPROM
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT6116 is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using IDT's high-performance, high-reliability technology — CEMOS™ II. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

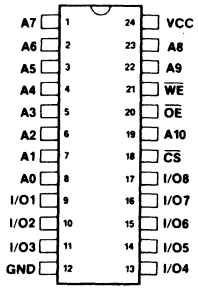
Address access times at 55 ns with chip select times as fast as 50 ns are available with maximum power consumption of only 550mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby power mode as long as $\overline{CS}$ remains high. In the standby mode, the low power device consumes less than 20μW typically. This capability provides significant system level power and cooling savings. Both versions also offer a battery backup data retention capability where the circuit typically consumes only 1μW to 4μW operating off of a 2V battery.

All inputs and outputs of the IDT6116 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

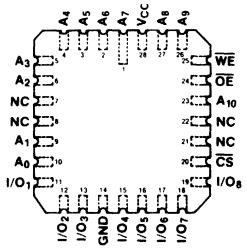
The IDT6116 is packaged in either a 24-pin, 600 and 300 mil-DIP or 32-pin and 28-pin leadless chip carriers, providing high board-level packing densities.

The IDT6116 Military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

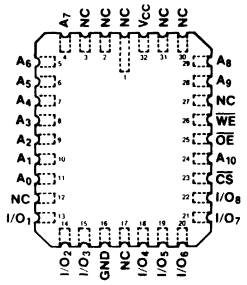
PIN CONFIGURATIONS



24 PIN SIDEBRAZE TOP VIEW

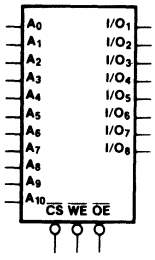


28 PIN LCC TOP VIEW



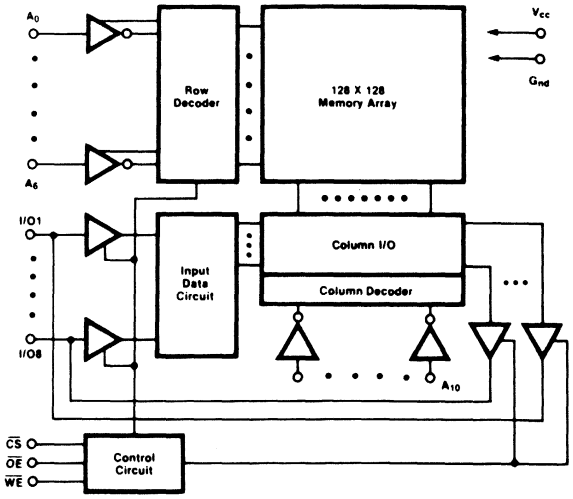
32 PIN LCC TOP VIEW

LOGIC SYMBOL



A_0-A_{10}	ADDRESS	$\overline{WE}$	WRITE ENABLE
I/O1-I/O8	DATA INPUT/OUTPUT	$\overline{OE}$	OUTPUT ENABLE
$\overline{CS}$	CHIP SELECT	GND	GROUND
V_{CC}	POWER		

FUNCTIONAL BLOCK DIAGRAM



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MILITARY, INDUSTRIAL, AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

ABSOLUTE MAXIMUM RATINGS(1)

TEMPERATURE RANGE		-55°C to +125°C	-40°C to +85°C	0°C to +70°C	
SYMBOL	PARAMETER	RATING			UNIT
V_{TERM}	Voltage on any Pin with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	-40 to +85	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	-55 to +125	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	-65 to +150	-10 to +85	°C
P_T	Power Dissipation	1.0	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	-.5(1)	—	+0.8	V
C_L	Output Load	—	—	100	pF
TTL	Output Load	—	—	1	—

MILITARY (T_A = -55°C to +125°C)
INDUSTRIAL (T_A = -40°C to +85°C)
COMMERCIAL (T_A = 0°C to +70°C)

NOTE:
1. V_{IL} min. = -3.0V for pulse width less than 20ns.

IDT6116S DC ELECTRICAL CHARACTERISTICS (V_{CC}= 5V ±10%, T_A= -55°C to +125°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6116S55/70/90			IDT6116S120			IDT6116S150			UNIT
			MIN.	TYP.(1)	MAX.	MIN.	TYP.(1)	MAX.	MIN.	TYP.(1)	MAX.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	10	—	—	10	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	—	—	10	—	—	10	—	—	10	µA
I_{CC}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	40	100	—	40	100	—	35	90	mA
I_{CC1}		V_{IH} = 3.5V, V_{IL} = 0.6V, $I_{I/O}$ = 0mA	—	35	—	—	35	—	—	30	—	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	40	100	—	40	100	—	35	90	mA
I_{SB}	Standby Power Current	$\overline{CS}$ = V_{IH}	—	5	25	—	5	25	—	5	25	mA
I_{SB1}		$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V	—	0.02	10	—	0.02	10	—	0.02	10	mA
V_{OL}	Output Low Voltage	I_{OL} = 3.5mA	—	—	0.4	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0mA	2.4	—	—	2.4	—	—	2.4	—	—	V

NOTE:
1. V_{CC} = 5V, T_A = 25°C.

IDT6116L DC ELECTRICAL CHARACTERISTICS (V_{CC}= 5V ±10%, T_A= -55°C to +125°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6116L55/70/90			IDT6116L120			IDT6116L150			UNIT
			MIN.	TYP.(1)	MAX.	MIN.	TYP.(1)	MAX.	MIN.	TYP.(1)	MAX.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	5	—	—	5	—	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	—	—	5	—	—	5	—	—	5	µA
I_{CC}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	40	100	—	35	90	—	30	80	mA
I_{CC1}		V_{IH} = 3.5V, V_{IL} = 0.6V, $I_{I/O}$ = 0mA	—	35	—	—	30	—	—	30	—	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	40	100	—	35	90	—	30	80	mA
I_{SB}	Standby Power Current	$\overline{CS}$ = V_{IH}	—	5	20	—	5	20	—	5	15	mA
I_{SB1}		$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V	—	4	900	—	4	900	—	4	900	µA
V_{OL}	Output Low Voltage	I_{OL} = 3.5mA	—	—	0.4	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0mA	2.4	—	—	2.4	—	—	2.4	—	—	V

NOTE:
1. V_{CC} = 5V, T_A = 25°C.

IDT6116S DC ELECTRICAL CHARACTERISTICS (V_{CC}= 5V ±10%, T_A= -40°C to +85°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6116S55/70			IDT6116S90/120			IDT6116S150			UNIT
			MIN.	TYP.(1)	MAX.	MIN.	TYP.(1)	MAX.	MIN.	TYP.(1)	MAX.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	10	—	—	10	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}	—	—	10	—	—	10	—	—	10	µA
I_{CC}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	40	100	—	40	90	—	35	80	mA
I_{CC1}		V_{IH} = 3.5V, V_{IL} = 0.6V $I_{I/O}$ = 0mA	—	35	—	—	35	—	—	30	—	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	40	100	—	40	90	—	35	80	mA
I_{SB}	Standby Power Current	$\overline{CS}$ = V_{IH}	—	5	20	—	5	20	—	5	20	mA
I_{SB1}		$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V	—	20	2000	—	20	2000	—	20	2000	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	—	0.4	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0mA	2.4	—	—	2.4	—	—	2.4	—	—	V

NOTE:
1. V_{CC} = 5V, T_A = 25°C.

IDT6116L DC ELECTRICAL CHARACTERISTICS (V_{CC}= 5V ±10%, T_A= -40°C to +85°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6116L55/70			IDT6116L90/120			IDT6116L150			UNIT
			MIN.	TYP.(1)	MAX.	MIN.	TYP.(1)	MAX.	MIN.	TYP.(1)	MAX.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	2	—	—	2	—	—	2	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}	—	—	2	—	—	2	—	—	2	µA
I_{CC}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	40	100	—	40/35	90/80	—	30	70	mA
I_{CC1}		V_{IH} = 3.5V, V_{IL} = 0.6V $I_{I/O}$ = 0mA	—	35	—	—	35/30	—	—	30	—	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	40	100	—	40/35	90/80	—	30	70	mA
I_{SB}	Standby Power Current	$\overline{CS}$ = V_{IH}	—	5	20	—	5	20/15	—	4	12	mA
I_{SB1}		$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V	—	4	200	—	4	200	—	4	200	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	—	0.4	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0mA	2.4	—	—	2.4	—	—	2.4	—	—	V

NOTE:
1. V_{CC} = 5V, T_A = 25°C.

IDT6116S DC ELECTRICAL CHARACTERISTICS (V_{CC}= 5V ±10%, GND = 0V, T_A= 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6116S55/70			IDT6116S90			IDT6116S120/150			UNIT
			MIN.	TYP.(1)	MAX.	MIN.	TYP.(1)	MAX.	MIN.	TYP.(1)	MAX.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	10	—	—	10	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}	—	—	10	—	—	10	—	—	10	µA
I_{CC}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	50	100	—	40	80	—	40	80	mA
I_{CC1}		V_{IH} = 3.5V, V_{IL} = 0.6V $I_{I/O}$ = 0mA	—	40	—	—	35	—	—	35	—	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	50	100	—	40	80	—	40	80	mA
I_{SB}	Standby Power Current	$\overline{CS}$ = V_{IH}	—	5	15	—	5	15	—	5	15	mA
I_{SB1}		$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V	—	20	2000	—	20	2000	—	20	2000	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	—	0.4	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0mA	2.4	—	—	2.4	—	—	2.4	—	—	V

NOTE:
1. V_{CC} = 5V, T_A = 25°C

IDT6116L DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, GND = 0V, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6116L55/70 MIN.	TYP.(1)	MAX.	IDT6116L90 MIN.	TYP.(1)	MAX.	IDT6116L120/150 MIN.	TYP.(1)	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	2	—	—	2	—	—	2	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}	—	—	2	—	—	2	—	—	2	µA
I_{CC}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	40	80	—	40	80	—	35/30	70/60	mA
I_{CC1}		V_{IH} = 3.5V, V_{IL} = 0.6V $I_{I/O}$ = 0mA	—	35	—	—	35	—	—	30	—	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	40	80	—	40	80	—	35/30	70/60	mA
I_{SB}	Standby Power Current	$\overline{CS}$ = V_{IH}	—	5	15	—	5	15	—	4	12	mA
I_{SB1}		$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V	—	4	100	—	4	100	—	4	100	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	—	0.4	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0mA	2.4	—	—	2.4	—	—	2.4	—	—	V

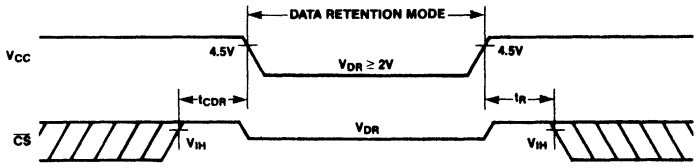
NOTE:
1. V_{CC} = 5V, T_A = 25°C.

DATA RETENTION CHARACTERISTICS (T_A = -55°C to +125°C/-40°C to +85°C/0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS		IDT6116L MIN.	TYP.(1)	MAX.	IDT6116S MIN.	TYP.(1)	MAX.	UNIT
V_{DR}	V_{CC} for Retention Data	V_{CC} = 2.0V, $\overline{CS}$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V		2.0	—	—	2.0	—	—	V
I_{CCDR}	Data Retention Current		COM'L	—	0.5	20	—	2	400	µA
			IND	—	0.5	40	—	2	600	µA
			MIL	—	0.5	300	—	2	1000	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	0	—	—	ns
t_R	Operation Recovery Time			t_{RC}(2)	—	—	t_{RC}(2)	—	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	1 TTL Gate and C_L = 100pF (including scope and jig)

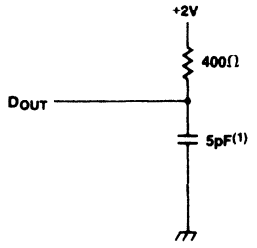


Figure 1. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

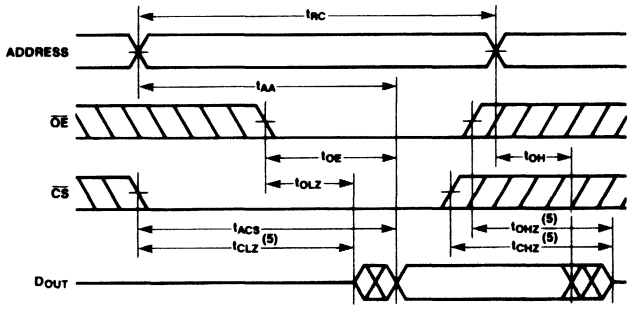
NOTE:
1. Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = -55°C to +125°C/-40°C to +85°C/0°C to +70°C)

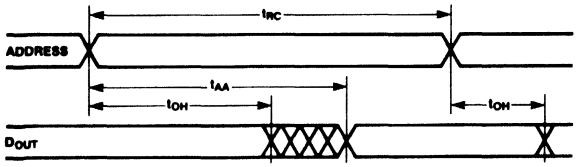
SYMBOL	PARAMETER	IDT6116S55 IDT6116L55 MIN.	MAX.	IDT6116S70 IDT6116L70 MIN.	MAX.	IDT6116S90 IDT6116L90 MIN.	MAX.	IDT6116S120 IDT6116L120 MIN.	MAX.	IDT6116S150 IDT6116L150 MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Access Time	55	—	70	—	90	—	120	—	150	—	ns
t_{AA}	Address Access Time	—	55	—	70	—	90	—	120	—	150	ns
t_{ACS}	Chip Select Access Time	—	50	—	65	—	90	—	120	—	150	ns
t_{CLZ}[1]	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	40	—	50	—	65	—	80	—	100	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselection to Output in High Z	0	30	0	35	0	40	0	40	0	50	ns
t_{OHZ}[1]	Output Disable to Output in High Z	0	30	0	35	0	40	0	40	0	50	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	55	—	70	—	90	—	120	—	150	—	ns
t_{CW}	Chip Selection to End of Write	40	—	40	—	55	—	70	—	90	—	ns
t_{AW}	Address Valid to End of Write	45	—	65	—	80	—	105	—	120	—	ns
t_{AS}	Address Setup Time	5	—	15	—	15	—	20	—	20	—	ns
t_{WP}	Write Pulse Width	40	—	40	—	55	—	70	—	90	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	5	—	5	—	10	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	0	30	0	35	0	40	0	40	0	50	ns
t_{WHZ}[1]	Write to Output in High Z	0	30	0	40	0	50	0	50	0	60	ns
t_{DW}	Data to Write Time Overlap	25	—	30	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	10	—	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter guaranteed but not tested.

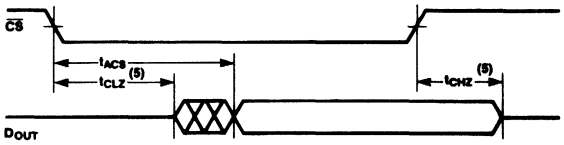
TIMING WAVEFORMS OF READ CYCLE NO. 1[1]



READ CYCLE 2[1,2,4]

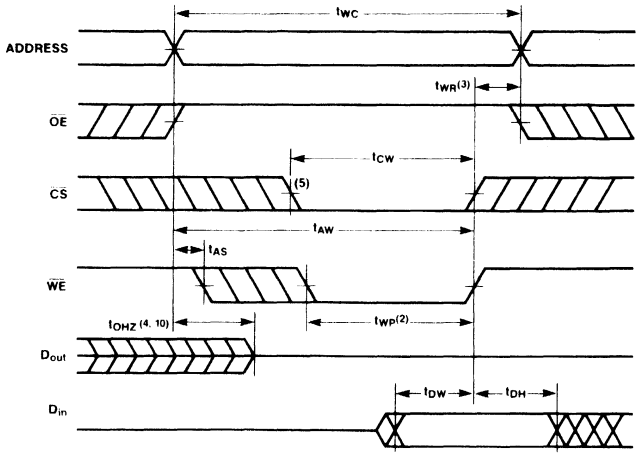


READ CYCLE 3[1,3,4]

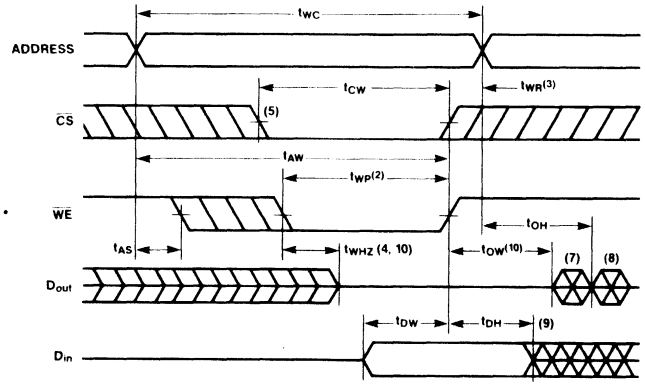


NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state with 5pF load (including scope and jig). This parameter is sampled and not 100% tested.

TIMING WAVEFORMS OF WRITE CYCLE 1(1)



TIMING WAVEFORM OF WRITE CYCLE 2(1,6)



NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{CE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O OPERATION
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Read	L	H	H	High Z
Write	L	X	L	D_{IN}

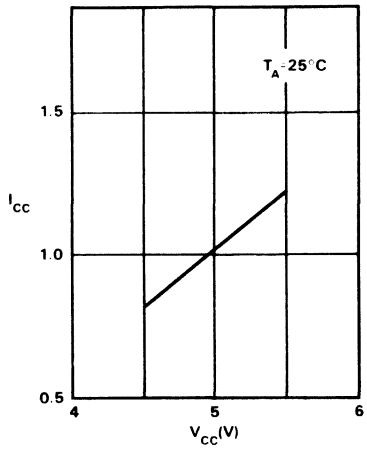
CAPACITANCE(1) (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

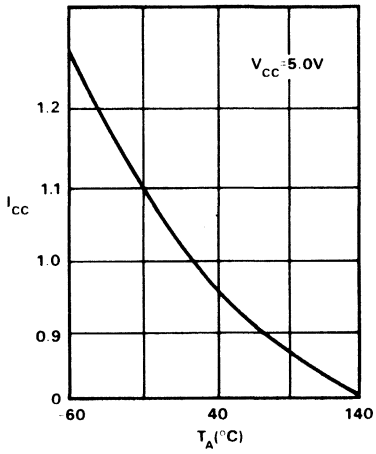
NOTE:
1. This parameter is sampled and not 100% tested.

NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

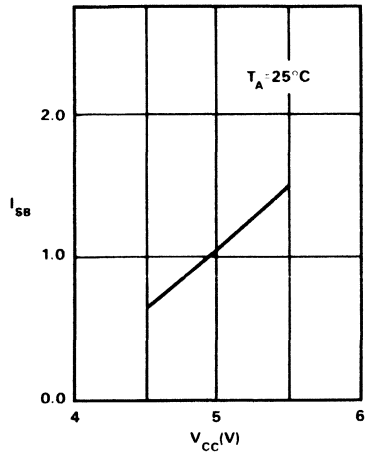
I_{CC} vs. Supply Voltage



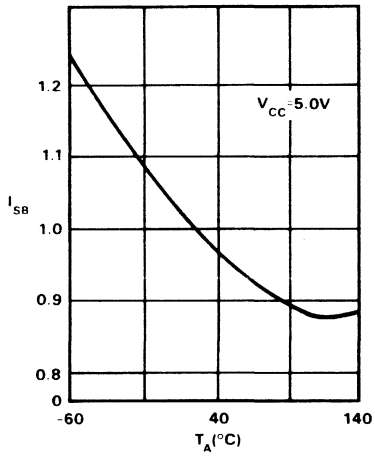
I_{CC} vs. Temperature



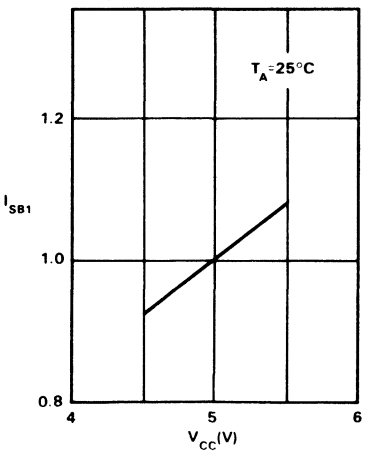
I_{SB} vs. Supply Voltage



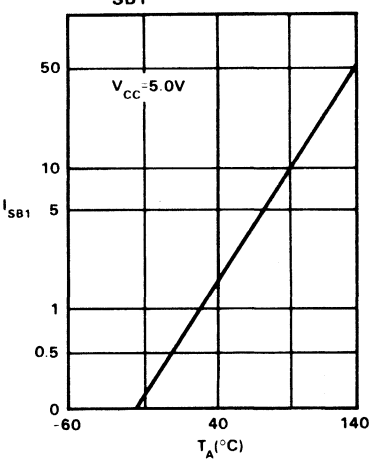
I_{SB} vs. Temperature



I_{SB1} vs. Supply Voltage

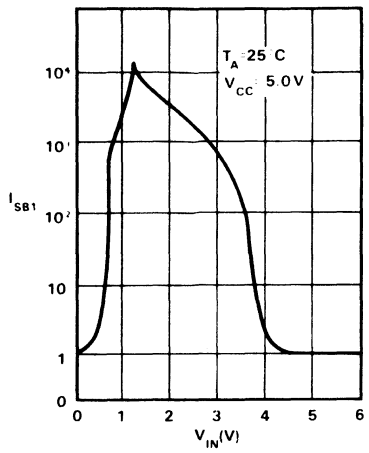


I_{SB1} vs. Temperature

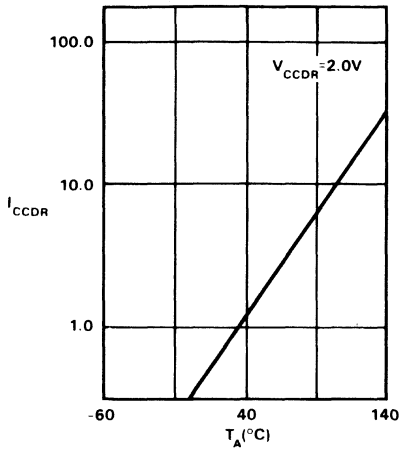


NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

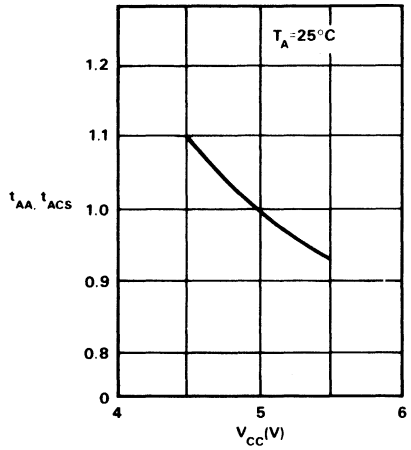
I_{SB1} vs. V_{IN}



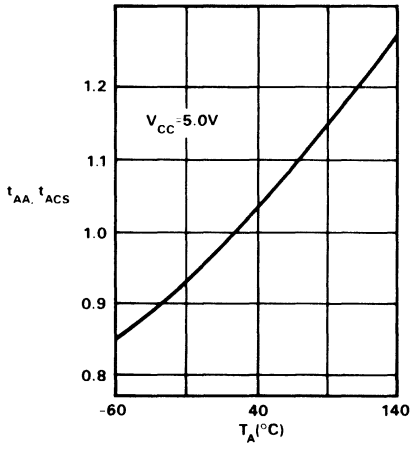
I_{CCDR} vs. Temperature



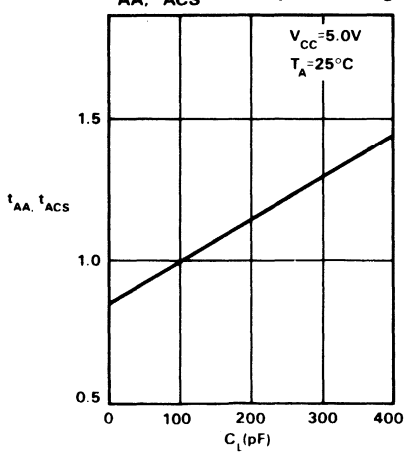
t_{AA}, t_{ACS} vs. Supply Voltage



t_{AA}, t_{ACS} vs. Temperature



t_{AA}, t_{ACS} vs. Output Loading



Integrated Device Technology, Inc.

CMOS STATIC RAMS 64K (64K x 1 BIT)

PRELIMINARY
IDT7187S
IDT7187L

FEATURES:

- High-speed (equal access and cycle time)
  - — Military/Industrial - 45/55/70/85ns (max.)
  - — Commercial - 35/45/55/70ns (max.)
- Low-power consumption
  - — IDT7187S
    - Active: 300mW (typ.)
    - Standby: 100μW (typ.)
  - — IDT7187L
    - Active: 250mW (typ.)
    - Standby: 30μW (typ.)
- Battery backup operation — 2V data retention (IDT7187L version only)
- JEDEC standard high-density 22-pin DIP and 28-pin leadless chip carrier
- Produced with advanced CEMOS™II high-performance technology
- Separate data input and output
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Pin compatible with standard 64Kx1 static RAMs
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

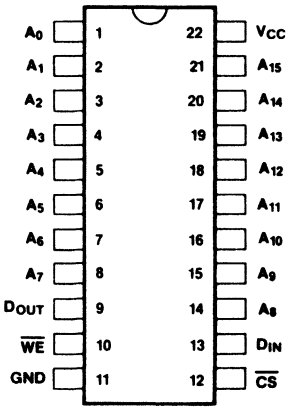
The IDT7187 is a 64K x 1 bit high-speed CEMOS™ II static RAM. It is available with 35, 45, 55, 70 or 85ns access times and consumes only 495mW maximum.

Both the standard (S) and low power (L) versions of the IDT7187 provide two standby modes - I_{SB} and I_{SB1}. I_{SB} provides low-power operation (192.5mW max.); I_{SB1} provides ultra low-power operation (5mW max.) The low power (L) version also provides the capability for data retention using battery backup. When using a 2V battery, the circuit typically consumes only 20μW.

Ease of system design is achieved by the IDT7187 with full asynchronous operation, along with matching access and cycle times. The device is packaged in an industry standard 22-pin, 300 mil DIP or 28-pin leadless chip carrier.

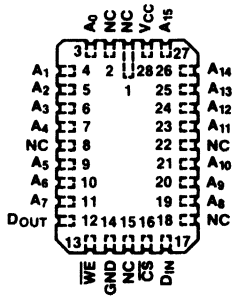
The IDT7187 military RAM version is 100% processed to the test methods of MIL-STD-883, Class B, Methods 5004 and 5005, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



SRD7187-001

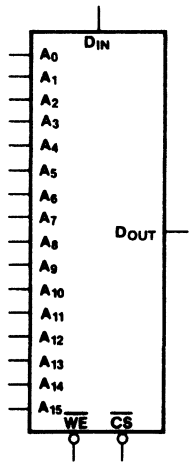
DIP
TOP VIEW



SRD7187-002

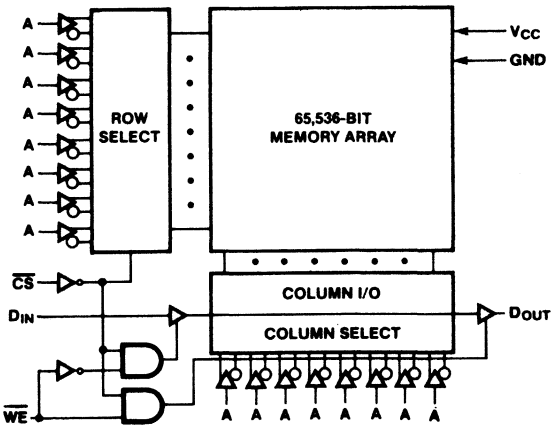
LCC
TOP VIEW

LOGIC SYMBOL



SRD7187-003

FUNCTIONAL BLOCK DIAGRAM



SRD7187-004

PIN NAMES

A_0 - A_{15}	ADDRESS INPUTS	D_{IN}	DATA IN
$\overline{CS}$	CHIP SELECT	D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE	GND	GROUND
V_{CC}	POWER		

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MILITARY, INDUSTRIAL, AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING		VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND		-0.5 to +7.0	V
T_A	Operating Temperature	COML. IND. MIL.	0 to +70 -40 to +85 -55 to +125	°C
T_{BIAS}	Temperature Under Bias		-65 to +135	°C
T_{STG}	Storage Temperature		-65 to +150	°C
P_T	Power Dissipation		1.0	W
I_{OUT}	DC Output Current		50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20 ns.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5.0V ± 10%, $V_{CC(min.)}$ = 4.5V, $V_{CC(max.)}$ = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7187S MIN.	IDT7187S TYP.(1)	IDT7187S MAX.	IDT7187L MIN.	IDT7187L TYP.(1)	IDT7187L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL. IND. COML.	— — —	— — —	10 10 5	— — —	— — —	5 5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. IND. COML.	— — —	— — —	10 10 5	— — —	— — —	5 5 2	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open V_{CC} = Max.	MIL. IND. COML.	— — —	60 60 60	120 120 110	— — —	50 50 50	100 100 90	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100% V_{CC} = Max., Output Open	MIL. IND. COML.	— — —	60 60 60	120 120 110	— — —	50 50 50	100 100 90	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$ V_{CC} = Max. Min. Duty Cycle = 100%	MIL. IND. COML.	— — —	30 30 30	50 50 45	— — —	25 25 25	40 40 35	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{HC}$, V_{CC} = Max. $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL. IND. COML.	— — —	.02 .02 .02	20 20 15	— — —	.006 .006 .006	2.7 2.7 0.9	mA
V_{OL}	Output Low Voltage	I_{OL} = 10mA V_{CC} = Min.		—	—	0.5	—	—	0.5	V
		I_{OL} = 8mA V_{CC} = Min.		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA V_{CC} = Min.		2.4	—	—	2.4	—	—	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

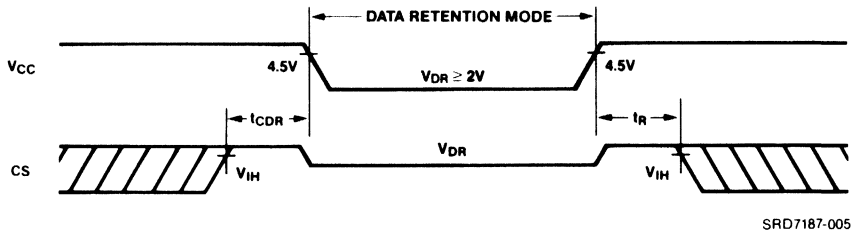
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC}@ 2.0V	TYP.(1) V_{CC}@ 3.0V	MAX. V_{CC}@ 2.0V	MAX. V_{CC}@ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL. IND. COML.	— — —	10 10 10	15 15 15	1000 1000 350	1500 1500 500	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—		—		ns
T_R	Operation Recovery Time			T_{RC}(2)	—		—		ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—		2		µA

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

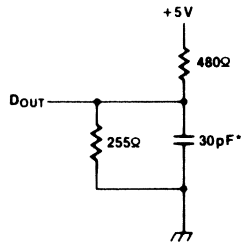


Figure 1. Output Load

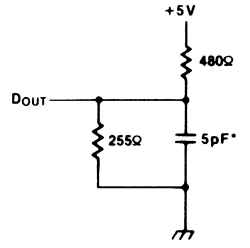


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

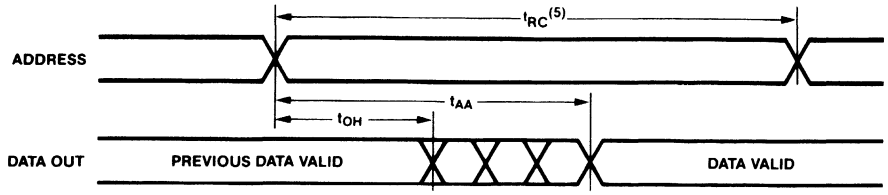
*Including scope and jig.

AC CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT7187S35(1) IDT7187L35(1) MIN.	MAX.	IDT7187S45 IDT7187L45 MIN.	MAX.	IDT7187S55 IDT7187L55 MIN.	MAX.	IDT7187S70 IDT7187L70 MIN.	MAX.	IDT7187S85(2) IDT7187L85(2) MIN.	MAX.	UNIT
READ CYCLE												
t_{RC} (TAVAV)	Read Cycle Time	35	—	45	—	55	—	70	—	85	—	ns
t_{AA} (TAVQV)	Address Access Time	—	35	—	45	—	55	—	70	—	85	ns
t_{ACS} (TELQV)	Chip Select Access Time	—	35	—	45	—	55	—	70	—	85	ns
t_{OH} (TAXQX)	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{LZ} (TELQX) (3)	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{HZ} (TEHQZ) (3)	Chip Deselection to Output in High Z	—	25	—	30	—	30	—	30	—	40	ns
t_{PU} (TELICCH) (3)	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD} (TEHICCL) (3)	Chip Selection to Power Down Time	—	30	—	35	—	35	—	35	—	40	ns
WRITE CYCLE												
t_{WC} (TAVAV)	Write Cycle Time	35	—	45	—	55	—	70	—	85	—	ns
t_{CW} (TELWH)	Chip Selection to End of Write	30	—	40	—	50	—	55	—	65	—	ns
t_{AW} (TAVWH)	Address Valid to End of Write	30	—	40	—	50	—	55	—	65	—	ns
t_{AS} (TAVWL)	Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP} (TWLWH)	Write Pulse Width	25	—	30	—	35	—	40	—	45	—	ns
t_{WR} (TWHAX)	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW} (TDVWH)	Data Valid to End of Write	20	—	25	—	25	—	30	—	35	—	ns
t_{DH} (TWHDX)	Data Hold Time	5	—	5	—	5	—	5	—	0	—	ns
t_{WZ} (TWLQZ) (3)	Write Enable to Output in High Z	0	25	0	30	0	30	0	30	0	40	ns
t_{OW} (TWHQZ) (3)	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

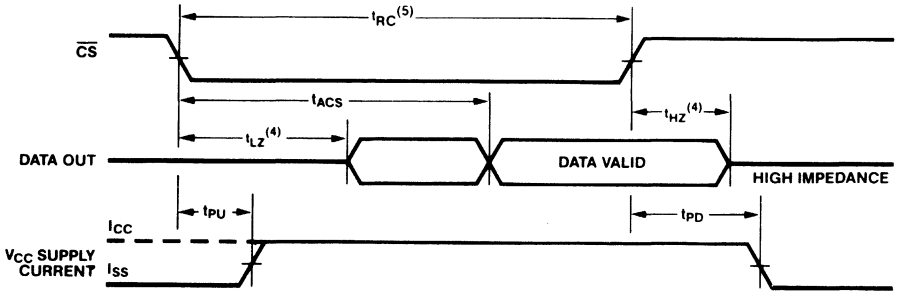
NOTES:
1. 0°C to +70°C only.
2. -40°C to +85°C and -55°C to +125°C only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1,2)



SRD7187-008

TIMING WAVEFORM OF READ CYCLE NO. (1, 3)

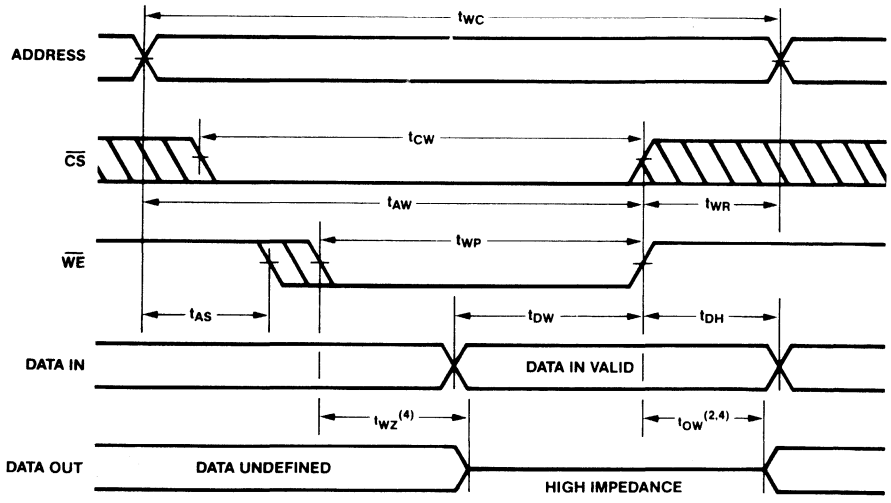


SRD7187-009

NOTES:

1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1)

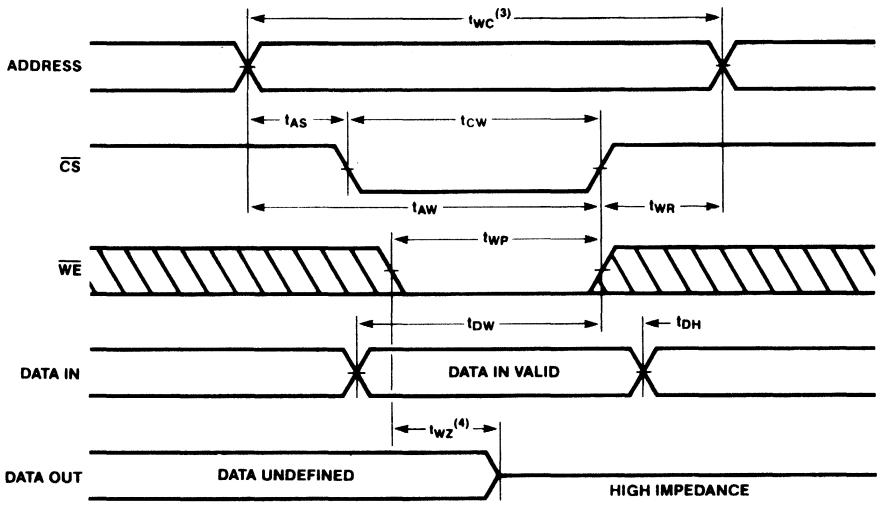


SRD7187-010

NOTES:

1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1)



SRD7187-011

NOTES:
1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

SYMBOL	ITEM	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
This parameter is sampled and not 100% tested.

Integrated Device Technology, Inc.

CMOS STATIC RAMS 64K (16K x 4 BIT)

IDT7188S
IDT7188L

FEATURES:

- High-speed (equal access and cycle times)
  - — Military/Industrial - 45/55/70/85ns max.
  - — Commercial - 45/55/70ns max.
- Low-power operation
  - — IDT7188S
    - Active: 350mW (typ.)
    - Standby: 100μW (typ.)
  - — IDT7188L
    - Active: 300mW (typ.)
    - Standby: 30μW (typ.)
- Battery backup operation — 2V data retention (L version only)
- High-density industry standard 22-pin, 300 mil DIP
- Produced with advanced CEMOS™II technology
- Bidirectional data inputs and outputs
- Single +5V (±10%) power supply
- Inputs/outputs TTL-compatible
- Three state outputs
- Static operation - no clocks or refresh required
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7188 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high reliability technology—CEMOS™II. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

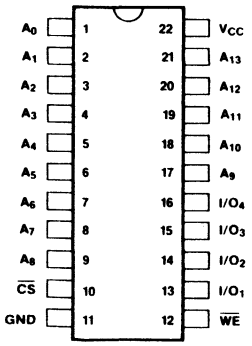
Access times as fast as 45ns are available, with maximum power consumption of only 605mW. The IDT7188 offers a reduced power standby mode, I_{SB1}, which enables the designer to greatly reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low power version (L) also offers a battery backup data retention capability where the circuit typically consumes only 20μW when operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5 volt supply. Fully static asynchronous circuitry, along with matching access and cycle times, favor the simplified system design approach.

The IDT7188 is packaged in a 22-pin, 300 mil DIP providing excellent board-level packing densities.

The IDT7188 military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

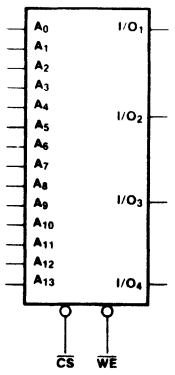
PIN CONFIGURATION



SSD7188-001

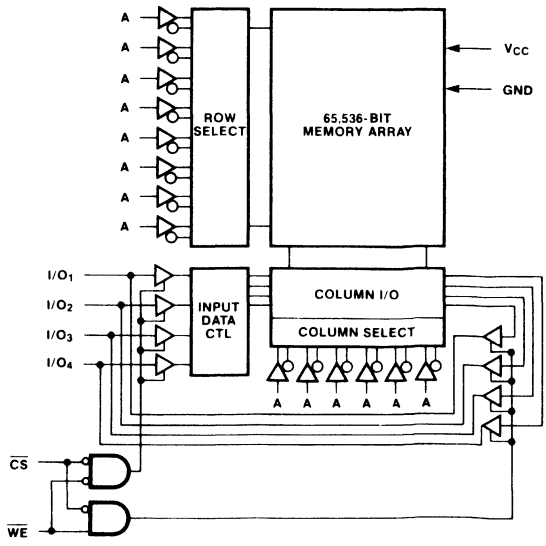
DIP
TOP VIEW

LOGIC SYMBOL



SSD7188-002

FUNCTIONAL BLOCK DIAGRAM



SSD7188-003

PIN NAMES

A_0-A_{13}	ADDRESS INPUTS	I/O_1-I/O_4	DATA I/O
$\overline{CS}$	CHIP SELECT	V_{CC}	POWER
$\overline{WE}$	WRITE ENABLE	GND	GROUND

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MILITARY, INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

*V_{IL} min = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5.0V ± 10%, $V_{CC(min.)}$ = 4.5V, $V_{CC(max.)}$ = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7188S MIN.	IDT7188S TYP.(1)	IDT7188S MAX.	IDT7188L MIN.	IDT7188L TYP.(1)	IDT7188L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL.	—	—	10	—	—	5	μA
			IND.	—	—	10	—	—	5	
			COM'L.	—	—	5	—	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	—	10	—	—	5	μA
			IND.	—	—	10	—	—	5	
			COM'L.	—	—	5	—	—	2	
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open V_{CC} = Max.	MIL.	—	70	140	—	60	125	mA
			IND.	—	70	140	—	60	125	
			COM'L.	—	70	125	—	60	110	
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100% V_{CC} = Max., Output Open	MIL.	—	85	140	—	75	125	mA
			IND.	—	85	140	—	75	125	
			COM'L.	—	85	125	—	75	110	
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$ V_{CC} = Max. Min. Duty Cycle = 100%	MIL.	—	30	50	—	25	40	mA
			IND.	—	30	50	—	25	40	
			COM'L.	—	30	45	—	25	35	
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{HC}$, V_{CC} = Max. $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	—	.02	20	—	.006	2.7	mA
			IND.	—	.02	20	—	.006	2.7	
			COM'L.	—	.02	15	—	.006	0.9	
V_{OL}	Output Low Voltage	I_{OL} = 10mA V_{CC} = Min.		—	—	0.5	—	—	0.5	V
		I_{OL} = 8mA V_{CC} = Min.		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA V_{CC} = Min.		2.4	—	—	2.4	—	—	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.

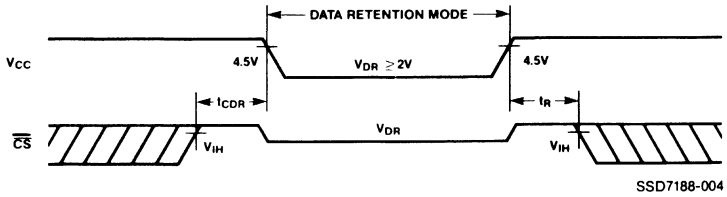
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC}@ 2.0V	TYP.(1) V_{CC}@ 3.0V	MAX. V_{CC}@ 2.0V	MAX. V_{CC}@ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	—	10	15	1000	1500	μA
			IND.	—	10	15	1000	1500	
			COML.	—	10	15	350	500	
t_{CDR}	Chip Deselect to Data Retention Time			0	—		—		ns
t_R	Operation Recovery Time			t_{RC}(2)	—		—		ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—		2		μA

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

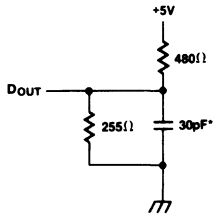
LOW V_{CC} DATA RETENTION WAVEFORM



SSD7188-004

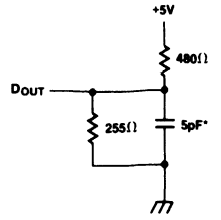
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2



SSD7188-005

Figure 1. Output Load



SSD7188-006

Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

***Including scope and jig.**

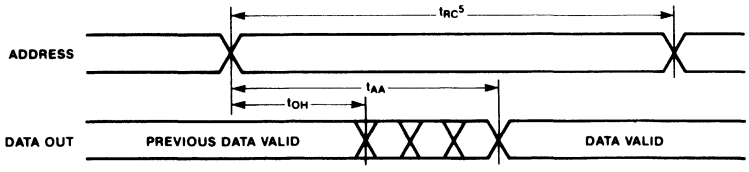
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, ALL TEMPERATURE RANGES)

SYMBOL	PARAMETER	IDT7188S45 IDT7188L45 MIN.	MAX.	IDT7188S55 IDT7188L55 MIN.	MAX.	IDT7188S70 IDT7188L70 MIN.	MAX.	IDT7188S85(1) IDT7188L85(1) MIN.	MAX.
READ CYCLE									
t_{RC}	Read Cycle Time	45	—	55	—	70	—	85	—
t_{AA}	Address Access Time	—	45	—	55	—	70	—	85
t_{ACS}	Chip Select Access Time	—	45	—	55	—	70	—	85
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—
t_{LZ}	Chip Selection to Output in Low Z(2)	5	—	5	—	5	—	5	—
t_{HZ}	Chip Deselection to Output in High Z(2)	—	15	—	20	—	25	—	30
t_{PU}	Chip Selection to Power Up Time(2)	0	—	0	—	0	—	0	—
t_{PD}	Chip Deselection to Power Down Time(2)	—	45	—	55	—	70	—	85
WRITE CYCLE									
t_{WC}	Write Cycle Time	40	—	50	—	60	—	75	—
t_{CW}	Chip Selection to End of Write	35	—	50	—	60	—	75	—
t_{AW}	Address Valid to End of Write	35	—	50	—	60	—	75	—
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—
t_{WP}	Write Pulse Width	35	—	50	—	60	—	75	—
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—
t_{DW}	Data Valid to End of Write	20	—	25	—	30	—	35	—
t_{DH}	Data Hold Time	5	—	5	—	5	—	5	—
t_{WZ}	Write Enable to Output in High Z(2)	—	15	—	25	—	30	—	40
t_{OW}	Output Active from End of Write	5	—	5	—	5	—	5	—

NOTE:

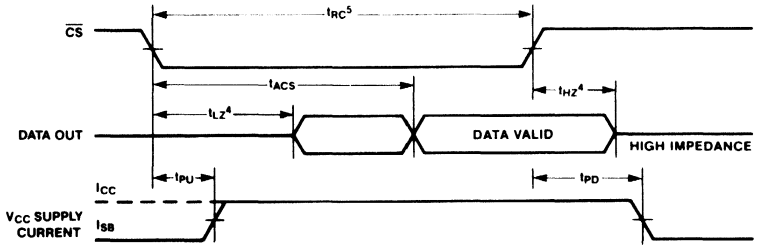
1. -40°C to +85°C and -55°C to +125°C product only.
2. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1,2)



SSD7188-007

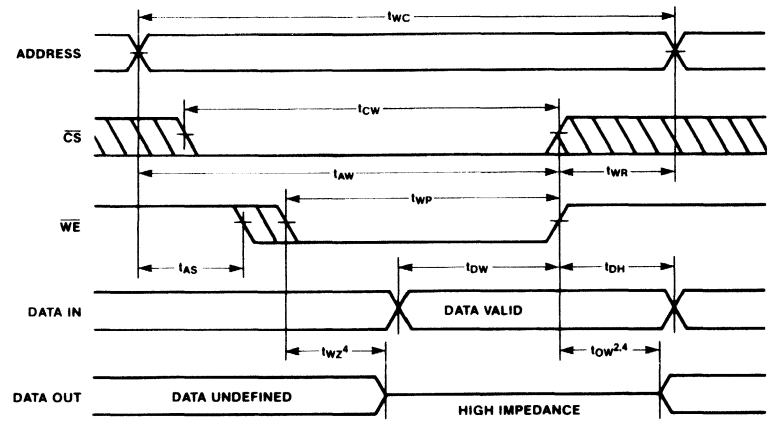
TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]



SSD7188-008

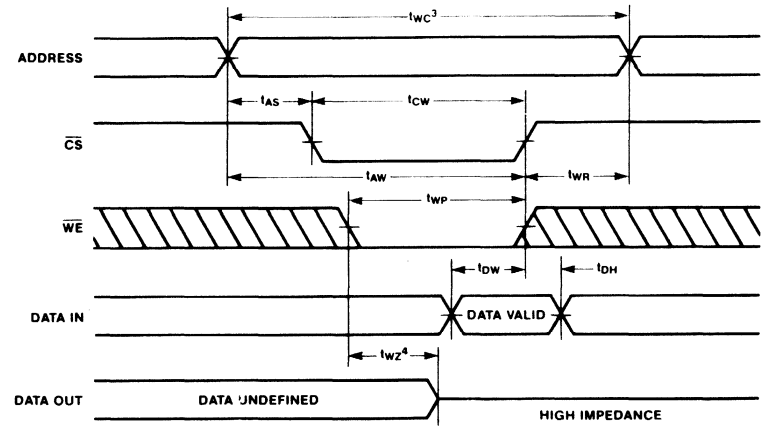
NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1]



SSD7188-009

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1]



SSD7188-010

NOTES:
1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.

Integrated Device Technology Inc

CMOS STATIC RAMS 64K (16K x 4 BIT)

Added chip select and output enable controls

IDT7198S
IDT7198L

FEATURES:

- Output Enable ($\overline{OE}$) pin available for added system flexibility
- Multiple Chip Selects ($\overline{CS_1}$, $\overline{CS_2}$) simplify system design and operation
- High-speed (equal access and cycle times)
  - — Military/Industrial—45/55/70/85ns max.
  - — Commercial—45/55/70ns max.
- Low-power operation
  - — IDT7198S
    - Active: 350mW (typ.)
    - Standby: 100μW (typ.)
  - — IDT7198L
    - Active: 300mW (typ.)
    - Standby: 30μW (typ.)
- Battery back-up operation — 2V data retention (L version only)
- 24-pin THINDIP and high-density 28-pin leadless chip carrier
- Produced with advanced CEMOS™II technology
- Bidirectional data inputs and outputs
- Military product 100% screened to MIL-STD-883, Class B

MEMORY CONTROL:

The IDT7198 64K high-speed CEMOS II static RAM incorporates two additional memory control features (an extra chip select and an output enable pin) which offer additional benefits in many system memory applications.

The dual chip select feature ($\overline{CS_1}$, $\overline{CS_2}$) now brings the convenience of improved system speeds to the large memory designer by reducing the external logic required to perform decoding. Since external decoding logic is reduced, board space is saved, system speed is enhanced by approximately 10-20ns and system reliability improves as a result of lower part count.

Both chip selects, chip select 1 ($\overline{CS_1}$) and chip select 2 ($\overline{CS_2}$), must be in the active-low state to select the memory. If either chip select is pulled high, the memory will be deselected and remain in the standby mode.

The output enable function ($\overline{OE}$) is also a highly desirable feature of the IDT7198 high-speed common I/O static RAM. This function is designed to eliminate problems associated with data bus contention by allowing the data outputs to be controlled independent of either chip select.

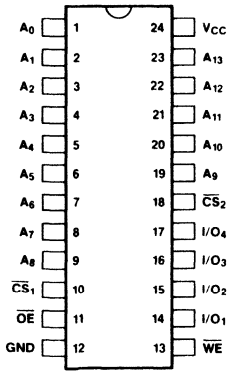
These added memory control features provide improved system design flexibility, along with overall system speed performance enhancements.

DESCRIPTION:

The IDT7198 is a 65,536 bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS™II. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

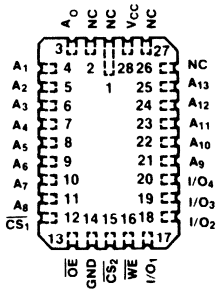
The IDT7198 features three memory control functions: chip select 1 ($\overline{CS_1}$), chip select 2 ($\overline{CS_2}$) and output enable ($\overline{OE}$). These three functions greatly enhance the IDT7198's overall flexibility in high-speed memory applications. **(Con't on next page)**

PIN CONFIGURATION



SRD7198-001

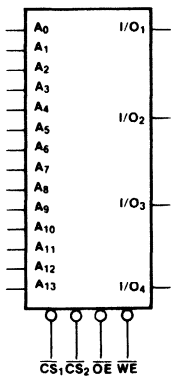
DIP
TOP VIEW



SRD7198-002

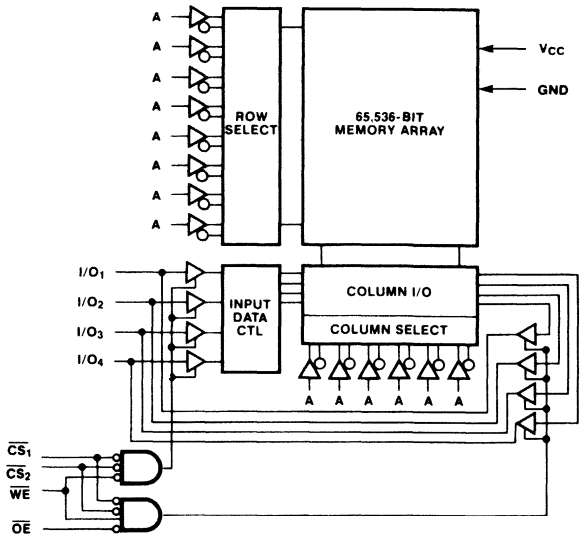
LCC
TOP VIEW

LOGIC SYMBOL



SRD7198-003

FUNCTIONAL BLOCK DIAGRAM



SRD7198-004

PIN NAMES

A_0-A_{13}	ADDRESS INPUTS	$\overline{OE}$	OUTPUT ENABLE
$\overline{CS_1}$	CHIP SELECT 1	I/O_1-I/O_4	DATA I/O
$\overline{CS_2}$	CHIP SELECT 2	V_{CC}	POWER
$\overline{WE}$	WRITE ENABLE	GND	GROUND

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MILITARY, INDUSTRIAL, AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

DESCRIPTION (Con't)

Access times as fast as 45ns are available with maximum power consumption of only 605mW. The IDT7198 offers a reduced power standby mode, I_{SB1}, which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low power version (L) also offers a battery backup data retention capability where the circuit typically consumes only 20μW when operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5 volt supply. Fully static asynchronous circuitry, along with matching access and cycle times, favor the simplified system design approach.

The IDT7198 is packaged in either a 24-pin dual in-line or 28-pin leadless chip carrier providing improved board-level packing densities.

The IDT7198 military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5*	—	0.8	V

*V_{IL} min = -3.0V for pulse width less than 20 ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5.0V ± 10%, $V_{CC(min.)}$ = 4.5V, $V_{CC(max.)}$ = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7198S MIN.	IDT7198S TYP.(1)	IDT7198S MAX.	IDT7198L MIN.	IDT7198L TYP.(1)	IDT7198L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL.	—	—	10	—	—	5	μA
			IND.	—	—	10	—	—	5	
			COM'L.	—	—	5	—	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	—	10	—	—	5	μA
			IND.	—	—	10	—	—	5	
			COM'L.	—	—	5	—	—	2	
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open V_{CC} = Max.	MIL.	—	70	140	—	60	125	mA
			IND.	—	70	140	—	60	125	
			COM'L.	—	70	125	—	60	110	
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100% V_{CC} = Max., Output Open	MIL.	—	85	140	—	75	125	mA
			IND.	—	85	140	—	75	125	
			COM'L.	—	85	125	—	75	110	
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} V_{CC} = Max. Min. Duty Cycle = 100%	MIL.	—	30	50	—	25	40	mA
			IND.	—	30	50	—	25	40	
			COM'L.	—	30	45	—	25	35	
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ ≥ V_{HC}, V_{CC} = Max. V_{IN} ≥ V_{HC} or ≤ V_{LC}	MIL.	—	.02	20	—	.006	2.7	mA
			IND.	—	.02	20	—	.006	2.7	
			COM'L.	—	.02	15	—	.006	0.9	
V_{OL}	Output Low Voltage	I_{OL} = 10mA V_{CC} = Min.		—	—	0.5	—	—	0.5	V
		I_{OL} = 8mA V_{CC} = Min.		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA V_{CC} = Min.		2.4	—	—	2.4	—	—	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

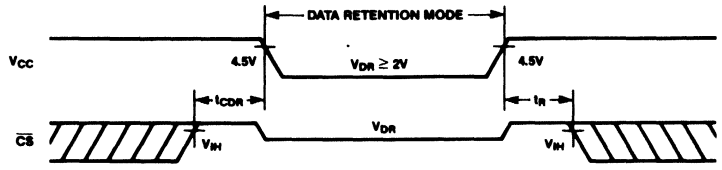
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC}@ 2.0V	TYP.(1) V_{CC}@ 3.0V	MAX. V_{CC}@ 2.0V	MAX. V_{CC}@ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	—	—	2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	—	10	15	1000	1500	µA
			IND.	—	10	15	1000	1500	
			COM'L.	—	10	15	350	500	
t_{CDR}	Chip Deselect to Data Retention Time			0			—		ns
t_R	Operation Recovery Time			t_{RC}(2)	—		—		ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—		2		µA

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



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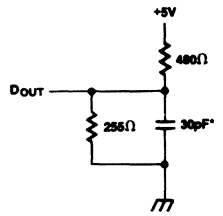
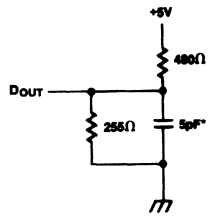
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2



SRD7198-006

Figure 1. Output Load



SRD7198-007

Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

***Including scope and jig**

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

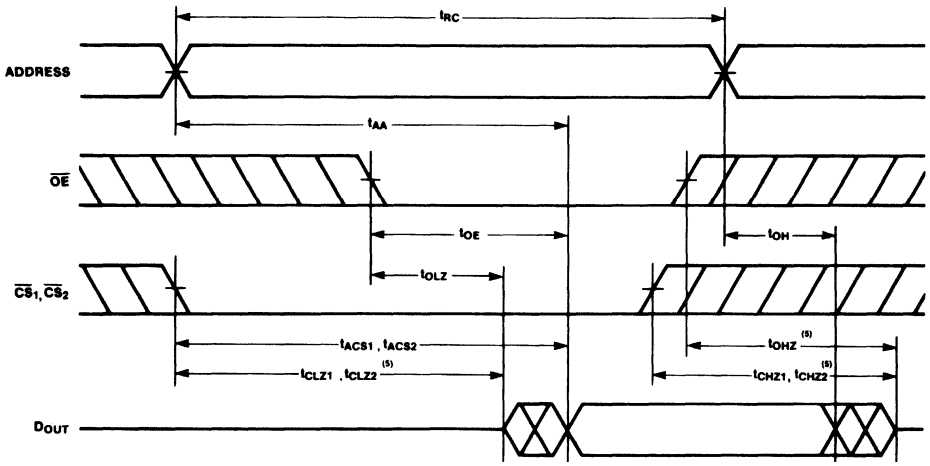
SYMBOL	PARAMETER	IDT7198S45 IDT7198L45 MIN.	IDT7198S45 IDT7198L45 MAX.	IDT7198S55 IDT7198L55 MIN.	IDT7198S55 IDT7198L55 MAX.	IDT7198S70 IDT7198L70 MIN.	IDT7198S70 IDT7198L70 MAX.	IDT7198S85(1) IDT7198L85(1) MIN.	IDT7198S85(1) IDT7198L85(1) MAX.	UNITS
READ CYCLE										
t_{RC}	Read Cycle Time	45	—	55	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	—	85	ns
$t_{ACS1,2}$	Chip Select-1, 2 Access Time(2)	—	45	—	55	—	70	—	85	ns
$t_{CLZ1,2}$(3)	Chip Select-1,2 to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	30	—	35	—	45	—	55	ns
t_{OLZ}(3)	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	ns
$t_{CHZ1,2}$(3)	Chip Select-1,2 to Output in High Z	—	15	—	20	—	25	—	30	ns
t_{OHZ}(3)	Output Disable to Output in High Z	—	15	—	20	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{PU}(3)	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(3)	Chip Deselection to Power Down Time	—	45	—	55	—	70	—	85	ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT7198S45 IDT7198L45 MIN.	MAX.	IDT7198S55 IDT7198L55 MIN.	MAX.	IDT7198S70 IDT7198L70 MIN.	MAX.	IDT7198S85[1] IDT7198L85[1] MIN.	MAX.	UNITS
WRITE CYCLE										
t_{WC}	Write Cycle Time	40	—	50	—	60	—	75	—	ns
$t_{CW1,2}$	Chip Selection to End of Write	35	—	50	—	60	—	75	—	ns
t_{AW}	Address Valid to End of Write	35	—	50	—	60	—	75	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	35	—	50	—	60	—	75	—	ns
$t_{WR1,2}$	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[3]	Write Enable to Output High Z	—	15	—	25	—	30	—	40	ns
t_{DW}	Data to Write Time Overlap	20	—	25	—	30	—	35	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	ns
t_{OW}[3]	Output Active from End of Write	5	—	5	—	5	—	5	—	ns

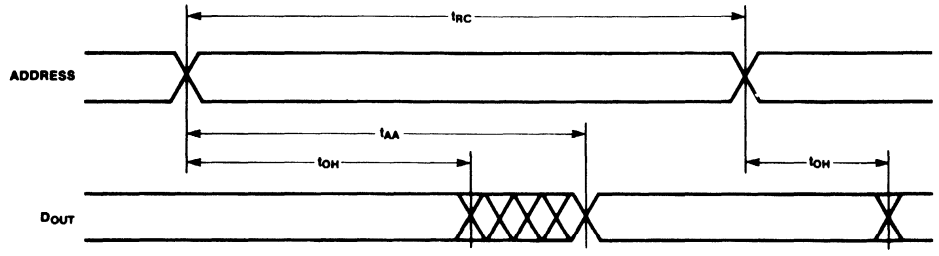
NOTES:
1. -40°C to +85°C and -55°C to +125°C product only.
2. Both chip selects must be active low for the device to be selected.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



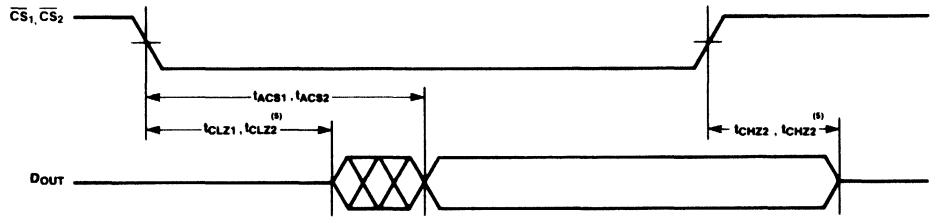
SRD7198-008

TIMING WAVEFORM OF READ CYCLE NO. 2[1,2,4]



SRD7198-009

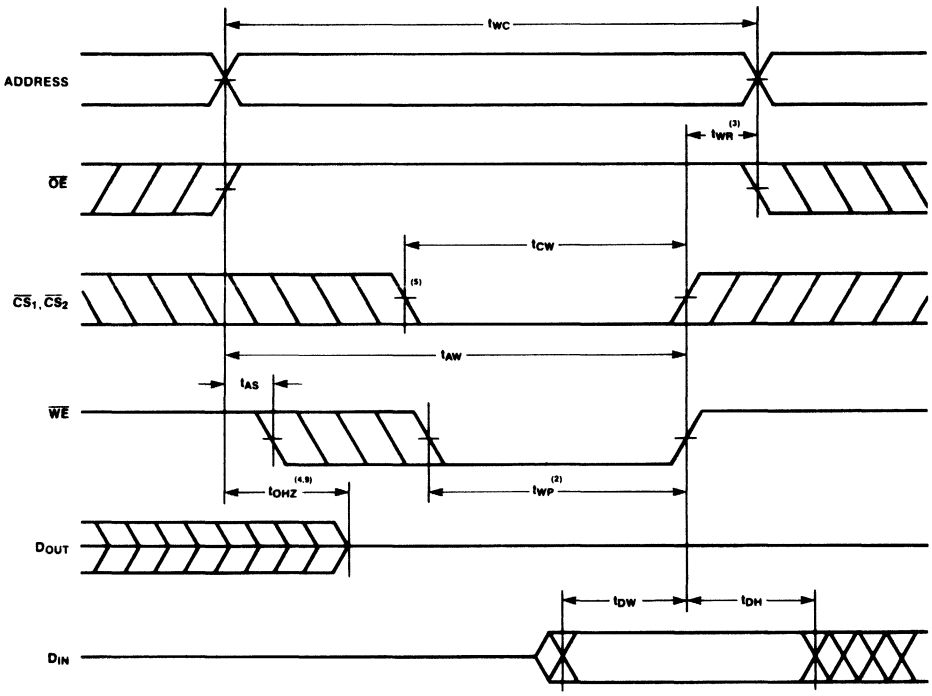
TIMING WAVEFORM OF READ CYCLE NO. 3[1,3,4]



SRD7198-010

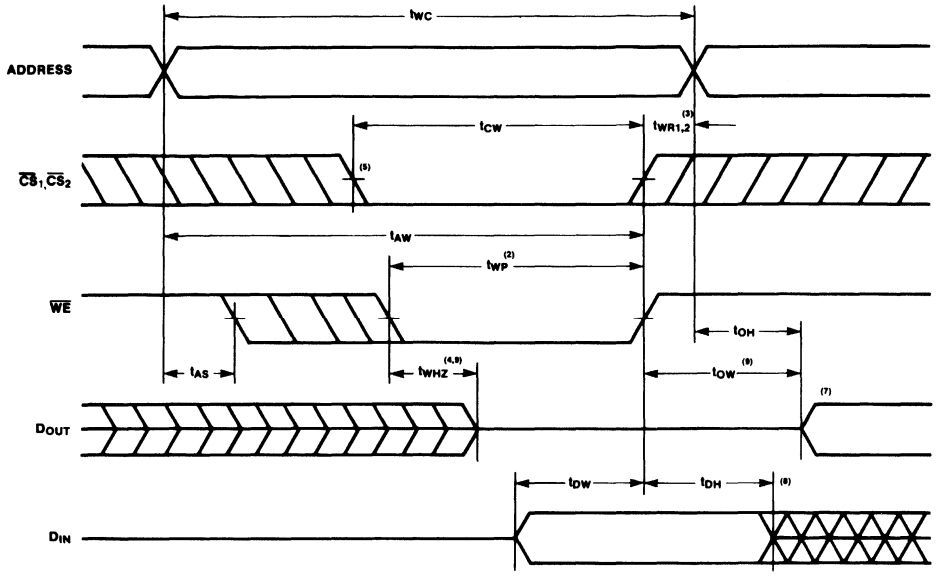
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS_1} = V_{IL}$, $\overline{CS_2} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS_1}$ and or $\overline{CS_2}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1[1]



SRD7198-011

TIMING WAVEFORM OF WRITE CYCLE NO. 2(1,6)



SRD7198-012

NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS_1}$ and a low $\overline{CS_2}$.
3. t_{WR} is measured from the earlier of $\overline{CS_1}$ or $\overline{CS_2}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS_1}$ and or $\overline{CS_2}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. If $\overline{CS_1}$ and $\overline{CS_2}$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TRUTH TABLE

MODE	$\overline{CS_1}$	$\overline{CS_2}$	$\overline{WE}$	$\overline{OE}$	OUTPUT	POWER
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	H	L	D_{OUT}	Active
Write	L	L	L	X	High Z	Active
Read	L	L	H	H	High Z	Active

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.

Integrated Device Technology, Inc.

CMOS STATIC RAMS 64K (16K x 4 BIT)

ADVANCE INFORMATION
IDT71981S/L
IDT71982S/L

SEPARATE DATA INPUTS AND OUTPUTS

FEATURES:

- Separate data inputs and outputs
- IDT71981S/L: outputs track inputs during write mode
- IDT71982S/L: high impedance outputs during write mode
- High-speed (equal access and cycle time)
  IDT7198/2S—45/55/70/85ns (max.)
  IDT7198/2L—45/55/70/85ns (max.)
- Low power consumption
  —IDT71981/2S
  Active: 350mW (Typ.)
  Standby: 100μW (Typ.)
  —IDT71981/2L
  Active: 300mW (Typ.)
  Standby: 30μW (Typ.)
- Battery backup operation—2V data retention (L version only)
- High-density 28-pin 600 mil dual in-line package and 28-pin leadless chip carriers
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT71981/IDT71982 are 65,536-bit high-speed static RAMs organized as 16K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

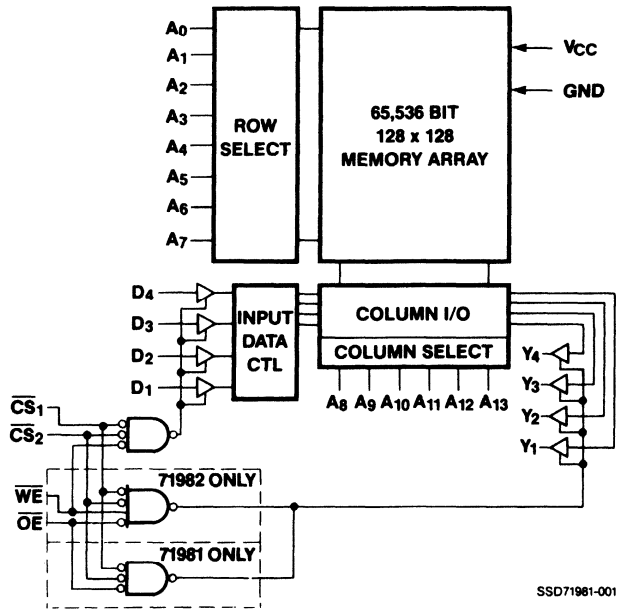
Access times as fast as 45ns are available with maximum power consumption of only 605mW. These circuits also offer a reduced power standby mode (I_{SB}). When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, this standby mode. In the ultra low power standby mode (I_{SB1}), the devices consume less than 30μW, typically. This capability provides significant system-level power and cooling savings. The low power (L) versions also offer a battery backup data retention capability where the circuit typically consumes only 20μW operating off a 2V battery.

All inputs and outputs of the IDT71981/IDT71982 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT71981/IDT71982 are packaged in either space-saving 28-pin, 600 mil DIPs or 28-pin leadless chip carriers, providing high board-level packing densities.

The IDT71981/IDT71982 Military RAMs are 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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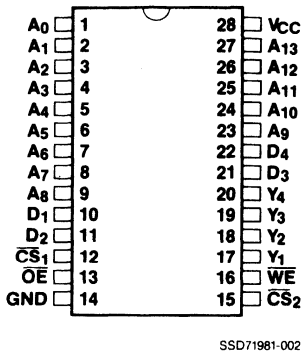
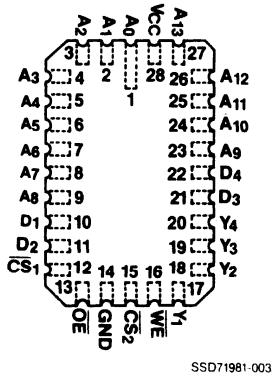
PIN CONFIGURATIONS

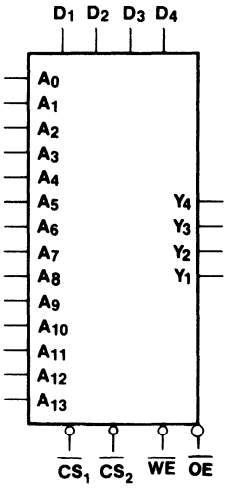


DIP
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_0-A_{13}	ADDRESS INPUTS	D_1-D_4	DATA IN
$\overline{CS}_1$, $\overline{CS}_2$	CHIP SELECTS	Y_1-Y_4	DATA OUT
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{OE}$	OUTPUT ENABLE	V_{CC}	POWER

Integrated Device Technology, Inc.

CMOS STATIC RAMS 64K (8K x 8 BIT)

ADVANCE INFORMATION
IDT7164S
IDT7164L

FEATURES:

- High-speed address/chip select access time
  - Military and Industrial—70ns (max.)
  - Commercial—55ns (max.)
- Low-power operation
  - —IDT7164S
    - Active: 300mW (typ.)
    - Standby: 100μW (typ.)
  - —IDT7164L
    - Active: 250mW (typ.)
    - Standby: 30μW (typ.)
- Battery Backup operation—2V data retention voltage
- Produced with advanced CEMOS™ II high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Standard 28-pin DIP and 32-pin LCC
- Pin compatible with standard 64K static RAM and EPROM
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7164 is a 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS™ II.

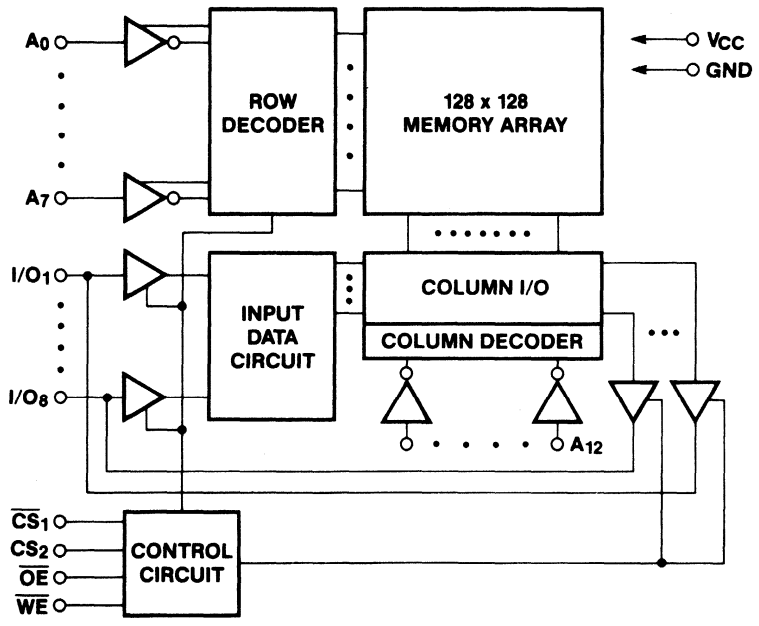
Address access times at 55ns are available with maximum power consumption of only 550mW. The circuit also offers a reduced power standby mode. When $\overline{CS}_1$ goes high or CS_2 goes low, the circuit will automatically go to, and remain in, a low power standby mode. In the full standby mode, the low power device consumes less than 30μW typically. Both versions also offer a battery backup data retention capability where the circuit typically consumes only 10μW operating off of a 2V battery.

All inputs and outputs of the IDT7164 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7164 is packaged in either a 28-pin, 600 mil-DIP or 32-pin leadless chip carrier, providing high board-level packing densities.

The IDT7164 Military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



SRD7164-001

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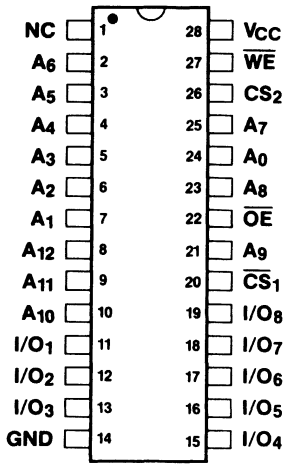
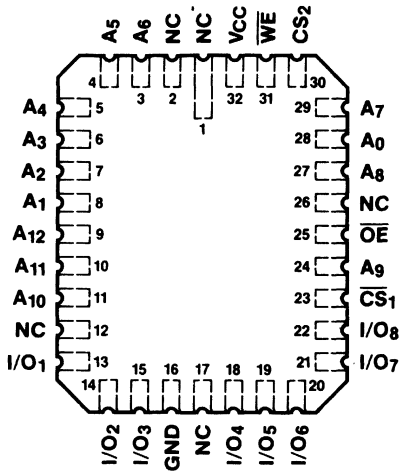
PIN CONFIGURATIONS



SRD7164-002

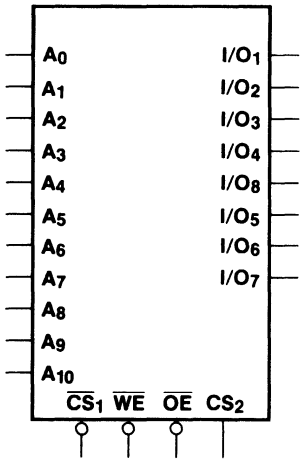
28 PIN SIDEBRAZE
TOP VIEW



SRD7164-003

32 PIN LCC
TOP VIEW

LOGIC SYMBOL



SRD7164-004

PIN NAMES

A_0-A_{10}	ADDRESS	$\overline{WE}$	WRITE ENABLE
I/O_1-I/O_8	DATA INPUT/OUTPUT	$\overline{OE}$	OUTPUT ENABLE
$\overline{CS_1}$	CHIP SELECT	GND	GROUND
CS_2	CHIP SELECT	V_{CC}	POWER

Integrated Device Technology Inc

CMOS DUAL PORT RAM 8K (1K x 8 BIT)

PRELIMINARY
IDT7130S
IDT7130L

FEATURES:

- High-speed access
  - —Military and Industrial
    100/120ns (max.)
  - —Commercial
    90/100ns (max.)
- Low-power operations
  - —IDT7130S
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - —IDT7130L
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- CEMOS™ II process virtually eliminates alpha particle induced soft-errors
- On-chip port arbitration logic
- $\overline{INT}$ and $\overline{BUSY}$ flags
- Fully asynchronous operation from either port
- Battery backup operation — 2V data retention
- Single 5V ± 10% power supply
- TTL compatibility
- Fully static operation
- Three state output
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

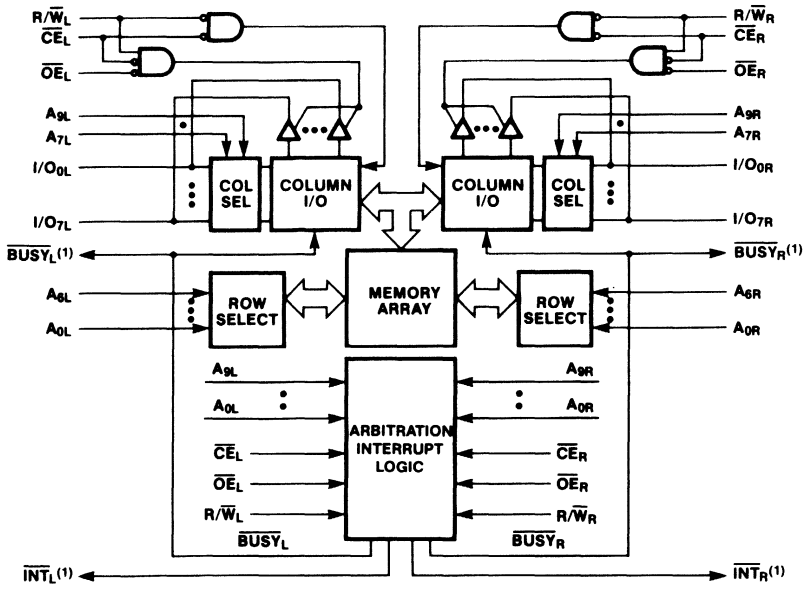
The IDT7130 is a CMOS 1Kx8 high-speed Dual Port Static RAM. It is fabricated using IDT's high-performance CEMOS II technology.

The IDT7130 provides two ports with separate controls, address and I/O that permit independent access for reads or writes to any location in memory. The IDT7130 has an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high).

Access times as fast as 90ns are available with typical operating power of only 325mW. The low power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 200μW off a 2V battery.

The IDT7130 is packaged in either a 48-pin DIP or a 48-pin leadless chip carrier. Military parts are 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



SRD7130-001

NOTE:
1. Open drain outputs: pullup resistor required.

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	CHIP ENABLE
R/$\overline{W}_L$	R/$\overline{W}_R$	READ/ WRITE ENABLE
$\overline{OE}_L$	$\overline{OE}_R$	OUTPUT ENABLE
$\overline{BUSY}_L$	$\overline{BUSY}_R$	BUSY FLAG
$\overline{INT}_L$	$\overline{INT}_R$	INTERRUPT FLAG
A_{0L}-A_{9L}	A_{0R}-A_{9R}	ADDRESS
I/O_{0L}-I/O_{7L}	I/O_{0R}-I/O_{7R}	DATA INPUT/ OUTPUT
V_{CC}		POWER
GND		GROUND

SRD7130-002

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MILITARY, INDUSTRIAL, AND COMMERCIAL TEMPERATURE RANGES

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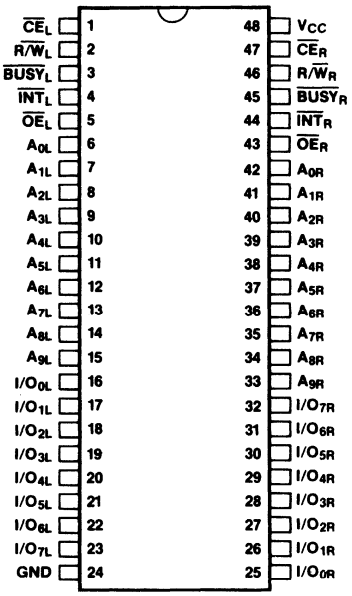
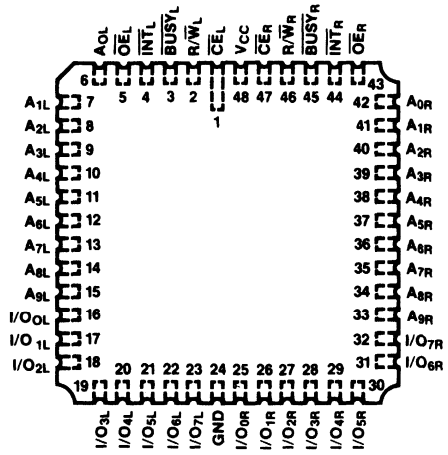
PIN CONFIGURATIONS



SRD7130-003

DIP
TOP VIEW



SRD7130-004

LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
MILITARY	-55°C to +125°C	0V	5.0V ± 10%
INDUSTRIAL	-40°C to +85°C	0V	5.0V ± 10%
COMMERCIAL	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = +5.0V ± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7130S MIN.	IDT7130S TYP.(1)	IDT7130S MAX.	IDT7130L MIN.	IDT7130L TYP.(1)	IDT7130L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}		—	—	10	—	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}		—	—	10	—	—	5	µA
V_{IH}	Input High Voltage			2.2	—	6.0	2.2	—	6.0	V
V_{IL}	Input Low Voltage			-1.0(2)	—	0.8	-1.0(2)	—	0.8	V
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open	COM'L.	—	65	170	—	65	120	mA
			IND.	—	65	180	—	65	140	
			MIL.	—	65	185	—	65	150	
I_{SB1}	Standby Current (Both Ports Standby)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$	COM'L.	—	25	40	—	25	30	mA
			IND.	—	25	50	—	25	40	
			MIL.	—	25	55	—	25	45	
I_{SB2}	Standby Current (One Port Standby)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open	COM'L.	—	40	110	—	40	75	mA
			IND.	—	40	120	—	40	90	
			MIL.	—	40	125	—	40	100	
I_{SB3}	Full Standby Current (Both Ports Full Standby)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V	COM'L.	—	1	15	—	0.2	4	mA
			IND.	—	1	25	—	0.2	8	
			MIL.	—	1	30	—	0.2	10	
I_{SB4}	Full Standby Current (One Port Full Standby)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open	COM'L.	—	40	90	—	35	65	mA
			IND.	—	40	100	—	35	75	
			MIL.	—	40	110	—	35	80	
V_{OL}	Output Low Voltage (I/O_0 - I/O_7)	I_{OL} = 3.5mA		—	—	0.4	—	—	0.4	V
		I_{OL} = 8mA		—	—	0.5	—	—	0.5	
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$, $\overline{INT}$)	I_{OL} = 16mA		—	—	0.5	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA		2.4	—	—	2.4	—	—	V

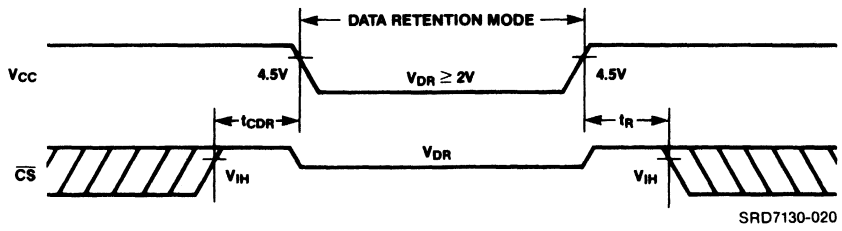
NOTES:
1. V_{CC} = 5V, T_A = +25°C.
2. V_{IL} min. = -3.5V for pulse width less than 30ns.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7130L MIN.	IDT7130L TYP.(1)	IDT7130L MAX.	UNIT
V_{DR}	V_{CC} for Retention Data	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V		2.0	—	—	V
I_{CCDR}	Data Retention Current		COM'L	—	100	1500	µA
			IND	—	100	3000	µA
			MIL	—	100	4000	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R	Operation Recovery Time			t_{RC}(2)	—	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.

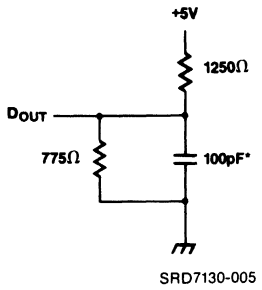
LOW V_{CC} DATA RETENTION WAVEFORM



SRD7130-020

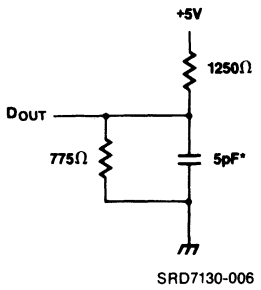
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, and 3



SRD7130-005

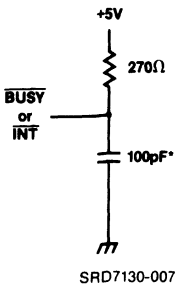
Figure 1. Output Load



SRD7130-006

Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

*Including scope and jig.



SRD7130-007

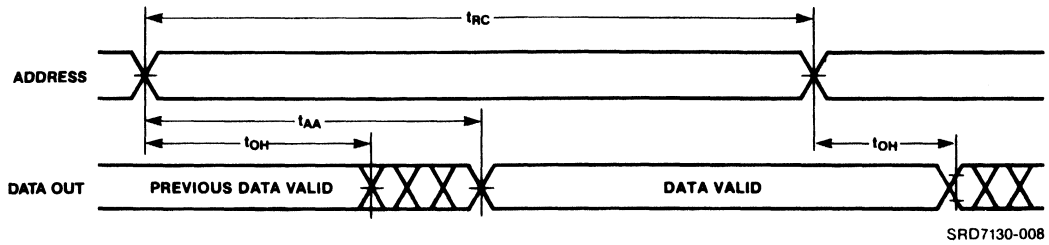
Figure 3. $\overline{BUSY}$ and $\overline{INT}$ Output Load

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

SYMBOL	PARAMETER	IDT7130S90(2) IDT7130L90 MIN.	MAX.	IDT7130S100 IDT7130L100 MIN.	MAX.	IDT7130S120(3) IDT7130L120 MIN.	MAX.	UNIT
READ CYCLE								
t_{RC}	Read Cycle Time	90	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	90	—	100	—	120	ns
t_{ACE}	Chip Enable Access Time	—	90	—	100	—	120	ns
t_{AOE}	Output Enable Access Time	—	40	—	40	—	60	ns
t_{OH}	Output Hold From Address Change	10	—	10	—	10	—	ns
t_{LZ}	Output Low Z Time(1,4)	5	—	5	—	5	—	ns
t_{HZ}	Output High Z Time(1,4)	—	40	—	40	—	40	ns
t_{PU}	Chip Enable to Power Up Time(4)	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time(4)	—	50	—	50	—	50	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	90	—	100	—	120	—	ns
t_{EW}	Chip Enable to End of Write	85	—	90	—	100	—	ns
t_{AW}	Address Valid to End of Write	85	—	90	—	100	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	60	—	60	—	70	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	40	—	40	—	40	—	ns
t_{HZ}	Output High Z Time(1,4)	—	40	—	40	—	40	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WZ}	Write Enabled to Output in High Z(1,4)	0	40	0	40	0	50	ns
t_{OW}	Output Active From End of Write(1,4)	0	—	0	—	0	—	ns
INTERRUPT TIMING								
t_{RC}	Read Cycle Time	90	—	100	—	120	—	ns
t_{WC}	Write Cycle Time	90	—	100	—	120	—	ns
t_{BAA}	$\overline{BUSY}$ Access Time to Address	—	45	—	50	—	60	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	—	45	—	50	—	60	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable	—	45	—	50	—	60	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Enable	—	45	—	50	—	60	ns
t_{APS}	Arbitration Priority Set Up Time	5	—	5	—	5	—	ns
BUSY TIMING								
t_{AS}	Address Set Up Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	55	—	60	—	70	ns
t_{INR}	Interrupt Reset Time	—	55	—	60	—	70	ns

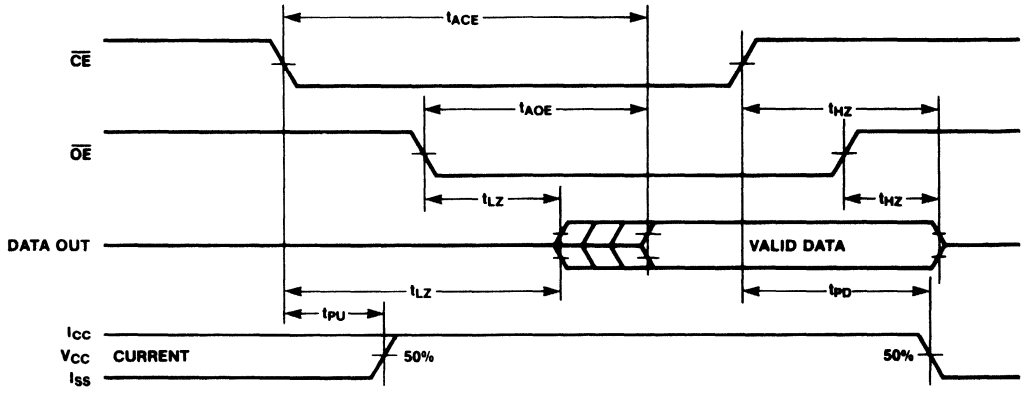
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 &3).
2. IDT7130S90 and IDT7130L90 available over T_A = 0°C to +70°C only.
3. IDT7130S120 and IDT7130L120 available over T_A, -40°C to +85°C and -55°C to +125°C only.
4. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1 EITHER SIDE(1,2,6)



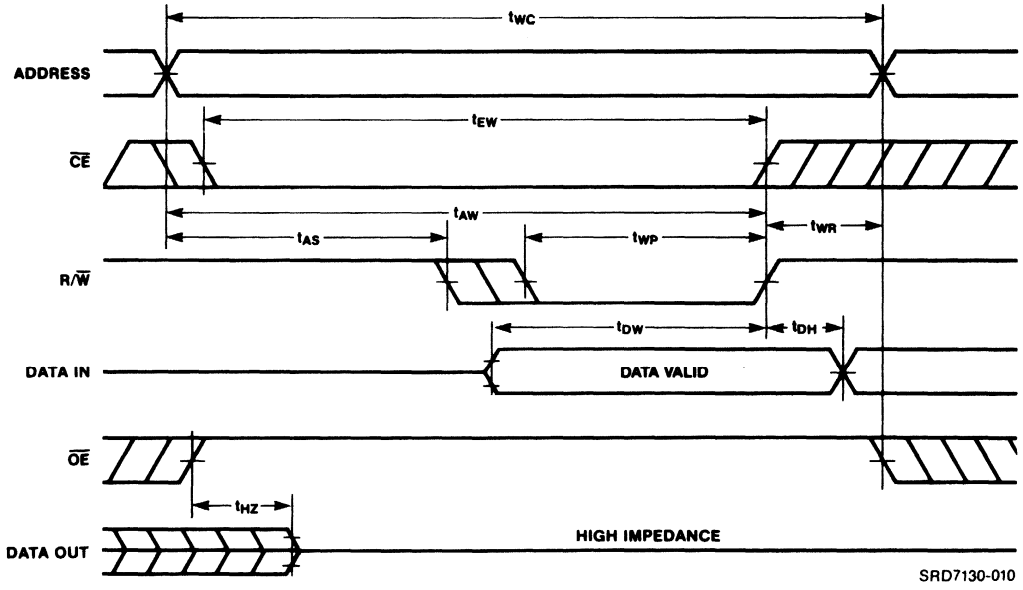
SRD7130-008

TIMING WAVEFORM OF READ CYCLE NO. 2 EITHER SIDE(1,3)



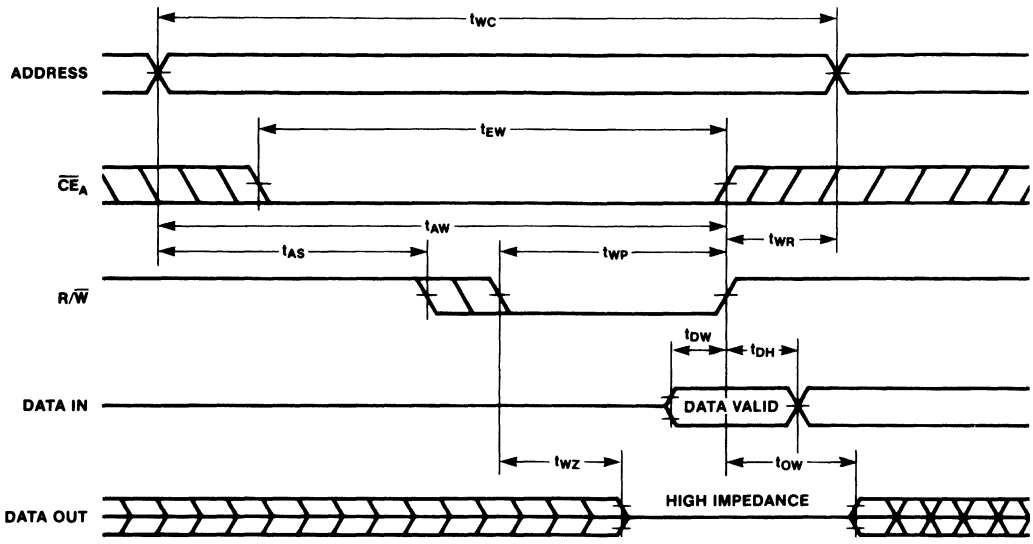
SRD7130-009

TIMING WAVEFORM OF WRITE CYCLE NO. 1 EITHER SIDE(4,7)



SRD7130-010

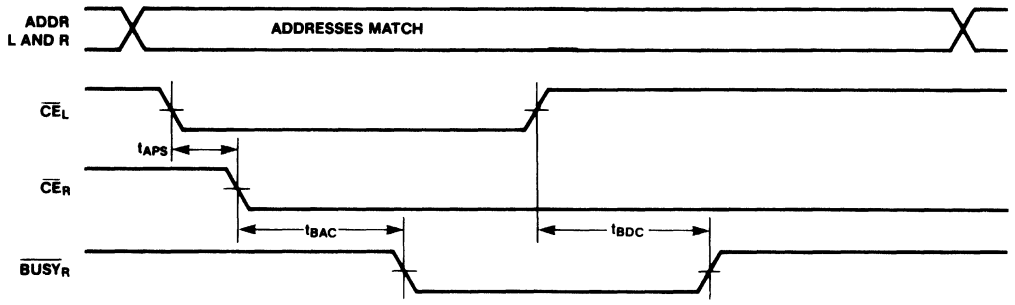
TIMING WAVEFORM OF WRITE CYCLE NO. 2 EITHER SIDE(4,7)



SRD7130-011

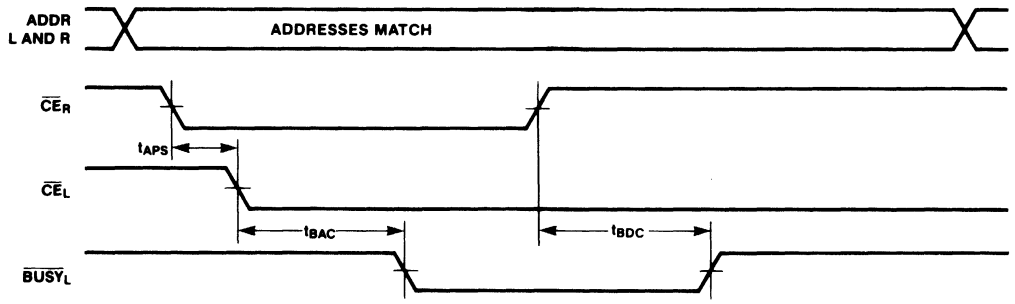
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1 $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:



SRD7130-013

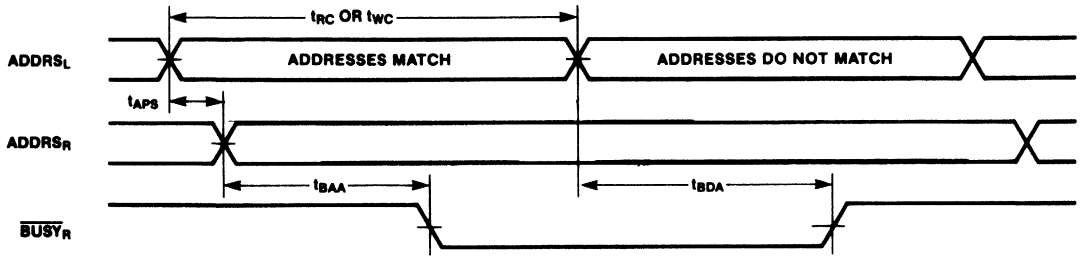
$\overline{CE}_R$ VALID FIRST



SRD7130-012

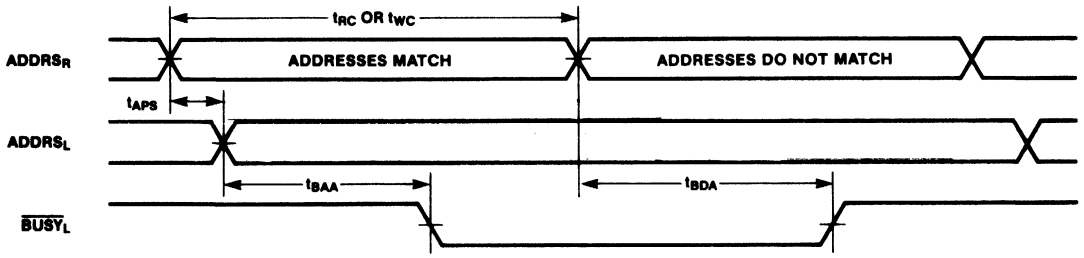
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2 ADDRESS VALID ARBITRATION[5]

LEFT ADDRESS VALID FIRST:



SRD7130-014

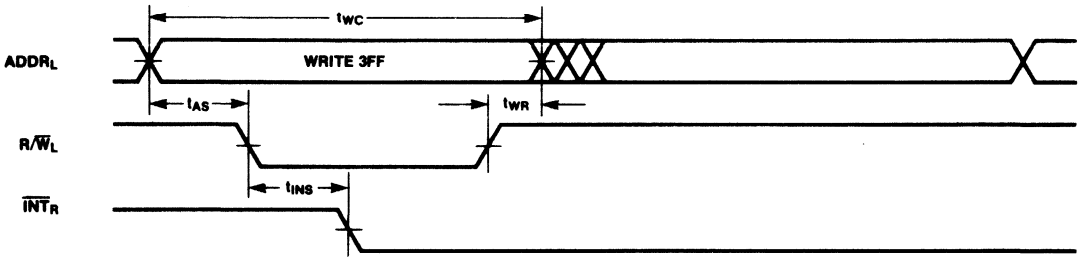
RIGHT ADDRESS VALID FIRST:



SRD7130-015

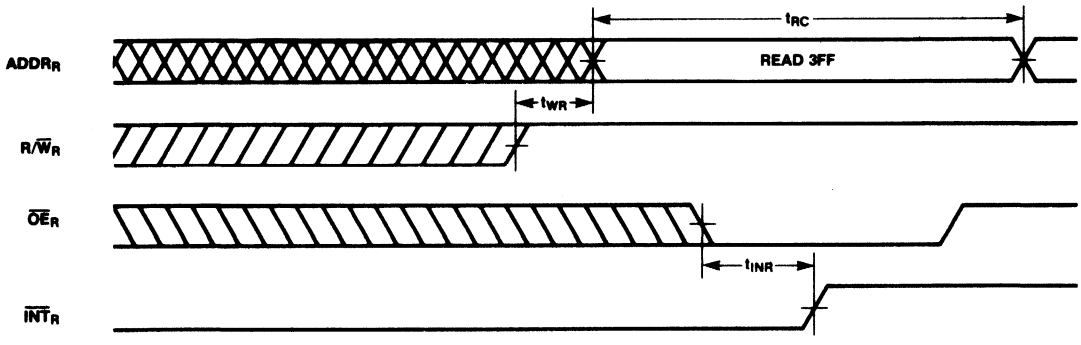
TIMING WAVEFORM OF INTERRUPT MODE[5,8]

LEFT SIDE SETS $\overline{INT}_R$:



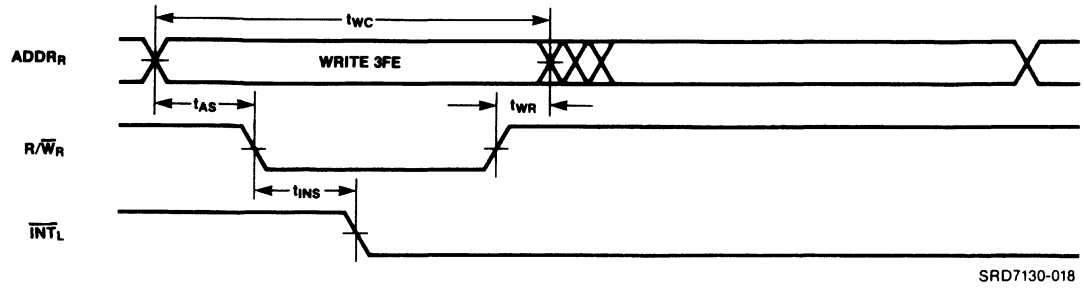
SRD7130-016

RIGHT SIDE CLEARS $\overline{INT}_R$:



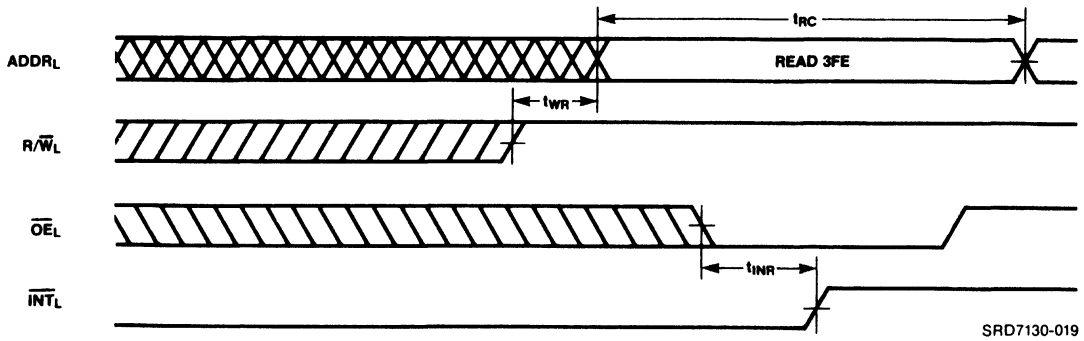
SRD7130-017

RIGHT SIDE SETS $\overline{INT}_L$:



SRD7130-018

LEFT SIDE CLEARS $\overline{INT}_L$:



SRD7130-019

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. If $\overline{CE}$ goes high simultaneously with R/$\overline{W}$ high, the outputs remain in the high impedance state.
5. $\overline{CE}_L$ = $\overline{CE}_R$ = V_{IL}.
6. $\overline{OE}$ = V_{IL}.
7. R/$\overline{W}$ = V_{IH} during address transition.
8. $\overline{INT}_R$ and $\overline{INT}_L$ are reset (high) during power up.

FUNCTIONAL DESCRIPTION:

The IDT7130 provides two ports with separate controls, address and I/O that permit independent access for reads or writes to any location in memory. The IDT7130 has an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

The interrupt flag ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 3FE (HEX). The left port clears the interrupt by reading address location 3FE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 3FF. The message (8-bits) at 3FE or 3FF is user-defined. If the interrupt function is not used, address locations 3FE and 3FF are not used as mail boxes but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access (refer to Table III, $\overline{CE}$ Arbitration); or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table IV, Address Arbitration). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

TRUTH TABLES

TABLE I — NON-CONTENTION READ/WRITE CONTROL

LEFT PORT INPUTS[1]			RIGHT PORT INPUTS [1]			FLAGS[2]		FUNCTION
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	H	X	X	X	X	H	H	Left Port in Power Down Mode
X	X	X	X	H	X	H	H	Right Port in Power Down Mode
L	L	X	X	X	X	H	H	Data on Left Port Written Into Memory
H	L	L	X	X	X	H	H	Data in Memory Output on Left Port
X	X	X	L	L	X	H	H	Data on Right Port Written Into Memory
X	X	X	H	L	L	H	H	Data in Memory Output on Right Port

NOTES:
1. $A_{0L} - A_{9L} \neq A_{0R} - A_{9R}$
2. $\overline{INT}$ Flags DON'T CARE
   H = HIGH, L = LOW, X = DON'T CARE

TABLE II — INTERRUPT FLAG

LEFT PORT					RIGHT PORT					FUNCTION
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{9L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{9R}	$\overline{INT}_R$	
L	L	X	3FF	X	X	X	X	X	L	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	H	L	L	3FF	H	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L	L	L	X	3FE	X	Set Left $\overline{INT}_L$ Flag
H	L	L	3FE	H	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTE:
H = HIGH, L = LOW, X = DON'T CARE

TABLE III — $\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$

LEFT PORT				RIGHT PORT				FLAGS[1]		FUNCTION
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{9L}	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{9R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	LBR	X	MATCH	X	L	X	MATCH	H	L	Left Operation Permitted Right Operation Not Permitted
X	L	X	MATCH	X	LBL	X	MATCH	L	H	Left Operation Not Permitted Right Operation Permitted
X	LST	X	MATCH	X	LST	X	MATCH	H	L	Arbitration Resolved

NOTE:
1. $\overline{INT}$ Flags DON'T CARE.
   X = DON'T CARE, L = LOW, H = HIGH, LST = Low Same Time, LBR = Low Before Right, LBL = Low Before Left.

TABLE IV — ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH

LEFT PORT				RIGHT PORT				FLAGS[1]		FUNCTION
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{9L}	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{9R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	L	X	VBR	X	L	X	VALID	H	L	Left Operation Permitted Right Operation Not Permitted
X	L	X	VALID	X	L	X	VBL	L	H	Left Operation Not Permitted Right Operation Permitted
X	L	X	VST	X	L	X	VST	H	L	Arbitration Resolved

NOTE:
1. $\overline{INT}$ Flags DON'T CARE.
   X = DON'T CARE, L = LOW, H = HIGH, LST = Low Same Time, LBR = Low Before Right, LBL = Low Before Left.

CAPACITANCE T_A = +25°C, f = 1.0MHz

SYMBOL	TEST	CONDITIONS	TYP.	UNIT
C_{OUT}	Output Capacitance	V_{IN} = 0V	10	pF
C_{IN}	Input Capacitance	V_{OUT} = 0V	10	pF

NOTE:
This parameter is sampled and not 100% tested.

Integrated Device Technology Inc

CMOS DUAL PORT RAM 16K (2K x 8 BIT)

PRELIMINARY
IDT7132S
IDT7132L

FEATURES:

- High-speed access
  - —Military and Industrial:
    100/120ns (max.)
  - —Commercial:
    90/100ns (max.)
- Low-power operations
  - —IDT7132S
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - —IDT7132L
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- CEMOS™ II process virtually eliminates alpha particle induced soft-errors
- On-chip port arbitration logic
- $\overline{BUSY}$ flags
- Fully asynchronous operation from either port
- Battery backup operation — 2V data retention
- Single 5V ± 10% power supply
- TTL compatibility
- Fully static operation
- Three state output
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

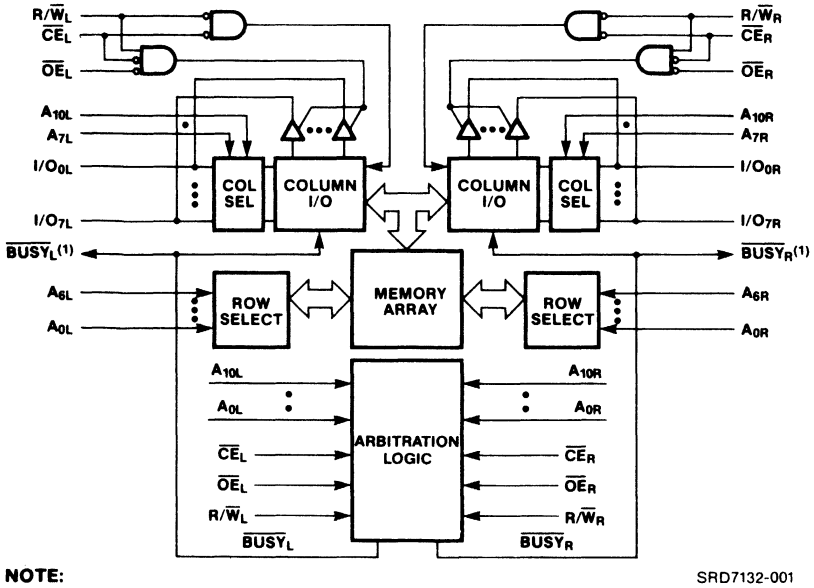
The IDT7132 is a CMOS 2Kx8 high-speed Dual Port Static RAM. It is fabricated using IDT's high-performance CEMOS II technology.

The IDT7132 provides two ports with separate controls, address and I/O that permit independent access for reads or writes to any location in memory. The IDT7132 has an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high).

Access times as fast as 90ns are available with typical operating power of only 325mW. The low power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 200μW off a 2V battery.

The IDT7132 is packaged in either a 48-pin DIP or a 48-pin leadless chip carrier. Military parts are 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



SRD7132-001

NOTE:
1. Open drain output: pull-up resistor required.

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	CHIP ENABLE
$R/\overline{W}_L$	$R/\overline{W}_R$	READ/ WRITE ENABLE
$\overline{OE}_L$	$\overline{OE}_R$	OUTPUT ENABLE
$\overline{BUSY}_L$	$\overline{BUSY}_R$	BUSY FLAG
A_{0L}-A_{10L}	A_{0R}-A_{10R}	ADDRESS
I/O_{0L}-I/O_{7L}	I/O_{0R}-I/O_{7R}	DATA INPUT/ OUTPUT
V_{CC}		POWER
GND		GROUND

SRD7132-002

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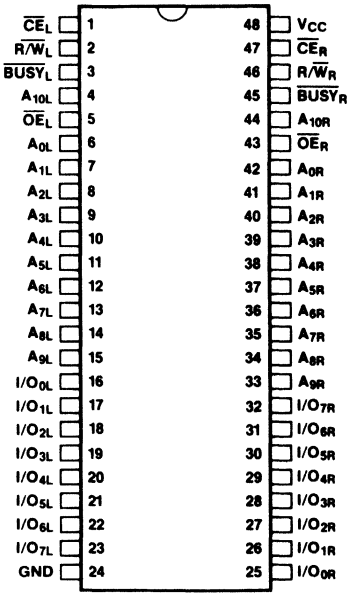
MILITARY, INDUSTRIAL, AND COMMERCIAL TEMPERATURE RANGES

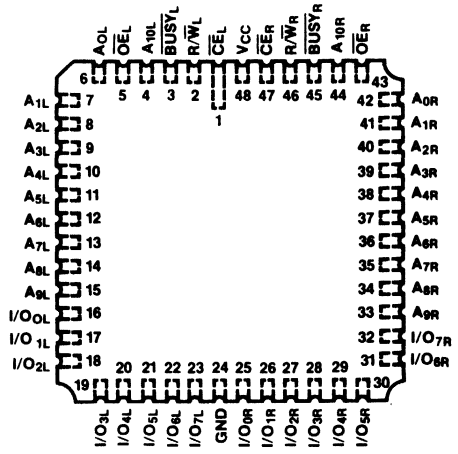
Printed in U.S.A.

PIN CONFIGURATIONS



SRD7132-003

DIP
TOP VIEW



SRD7132-004

LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
MILITARY	-55°C to +125°C	0V	5.0V ± 10%
INDUSTRIAL	-40°C to +85°C	0V	5.0V ± 10%
COMMERCIAL	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7132S MIN.	IDT7132S TYP.(1)	IDT7132S MAX.	IDT7132L MIN.	IDT7132L TYP.(1)	IDT7132L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}		—	—	10	—	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}		—	—	10	—	—	5	µA
V_{IH}	Input High Voltage			2.2	—	6.0	2.2	—	6.0	V
V_{IL}	Input Low Voltage			-1.0(2)	—	0.8	-1.0(2)	—	0.8	V
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open	COM'L.	—	65	170	—	65	120	mA
			IND.	—	65	180	—	65	140	
			MIL.	—	65	185	—	65	150	
I_{SB1}	Standby Current (Both Ports Standby)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$	COM'L.	—	25	50	—	25	30	mA
			IND.	—	25	60	—	25	40	
			MIL.	—	25	65	—	25	45	
I_{SB2}	Standby Current (One Port Standby)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open	COM'L.	—	40	110	—	40	75	mA
			IND.	—	40	120	—	40	90	
			MIL.	—	40	125	—	40	100	
I_{SB3}	Full Standby Current (Both Ports Full Standby)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V	COM'L.	—	1	15	—	0.2	4	mA
			IND.	—	1	25	—	0.2	8	
			MIL.	—	1	30	—	0.2	10	
I_{SB4}	Full Standby Current (One Port Full Standby)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open	COM'L.	—	40	90	—	35	65	mA
			IND.	—	40	100	—	35	75	
			MIL.	—	40	110	—	35	80	
V_{OL}	Output Low Voltage (I/O_0 - I/O_7)	I_{OL} = 3.5mA		—	—	0.4	—	—	0.4	V
		I_{OL} = 8mA		—	—	0.5	—	—	0.5	
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA		—	—	0.5	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA		2.4	—	—	2.4	—	—	V

NOTES:
1. V_{CC} = 5V, T_A = +25°C.
2. V_{IL} min. = -3.5V for pulse width less than 30ns.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

SYMBOL	PARAMETER	IDT7132S90(2) IDT7132L90 MIN.	IDT7132S90(2) IDT7132L90 MAX.	IDT7132S100 IDT7132L100 MIN.	IDT7132S100 IDT7132L100 MAX.	IDT7132S120(3) IDT7132L120 MIN.	IDT7132S120(3) IDT7132L120 MAX.	UNIT
READ CYCLE								
t_{RC}	Read Cycle Time	90	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	90	—	100	—	120	ns
t_{ACE}	Chip Enable Access Time	—	90	—	100	—	120	ns
t_{AOE}	Output Enable Access Time	—	40	—	40	—	60	ns
t_{OH}	Output Hold From Address Change	10	—	10	—	10	—	ns
t_{LZ}	Output Low Z Time (1,4)	5	—	5	—	5	—	ns
t_{HZ}	Output High Z Time (1,4)	—	40	—	40	—	40	ns
t_{PU}	Chip Enable to Power Up Time (4)	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time (4)	—	50	—	50	—	50	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	90	—	100	—	120	—	ns
t_{EW}	Chip Enable to End of Write	85	—	90	—	100	—	ns
t_{AW}	Address Valid to End of Write	85	—	90	—	100	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	60	—	60	—	70	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	40	—	40	—	40	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{HZ}	Output High Z Time(1,4)	—	40	—	40	—	40	ns
t_{WZ}	Write Enabled to Output in High Z (1,4)	0	40	0	40	0	50	ns
t_{OW}	Output Active From End of Write (1,4)	0	—	0	—	0	—	ns

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (Cont'd)

SYMBOL	PARAMETER	IDT7130S90[2] IDT7130L90 MIN.	MAX.	IDT7130S100 IDT7130L100 MIN.	MAX.	IDT7130S120[3] IDT7130L120 MIN.	MAX.	UNIT
BUSY TIMING								
t_{RC}	Read Cycle Time	90	—	100	—	120	—	ns
t_{WC}	Write Cycle Time	90	—	100	—	120	—	ns
t_{BAA}	$\overline{BUSY}$ Access Time to Address	—	45	—	50	—	60	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	—	45	—	50	—	60	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable	—	45	—	50	—	60	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Enable	—	45	—	50	—	60	ns
t_{APS}	Arbitration Priority Set Up Time	5	—	5	—	5	—	ns

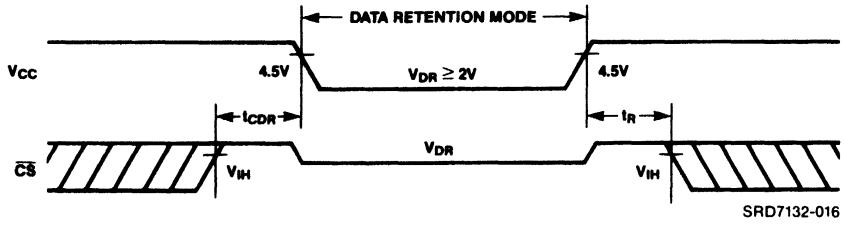
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 &3).
2. IDT7132S90 and IDT7132L90 available over T_A = 0°C to +70°C only.
3. IDT7132S120 and IDT7132L120 available over T_A, -40°C to +85°C and -55°C to +125°C only.
4. This parameter guaranteed but not tested.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7132L MIN.	TYP.[1]	MAX.	UNIT
V_{DR}	V_{CC} for Retention Data	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V		2.0	—	—	V
I_{CCDR}	Data Retention Current		COM'L	—	100	1500	µA
			IND	—	100	3000	µA
			MIL	—	100	4000	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R	Operation Recovery Time			t_{RC}[2]	—	—	ns

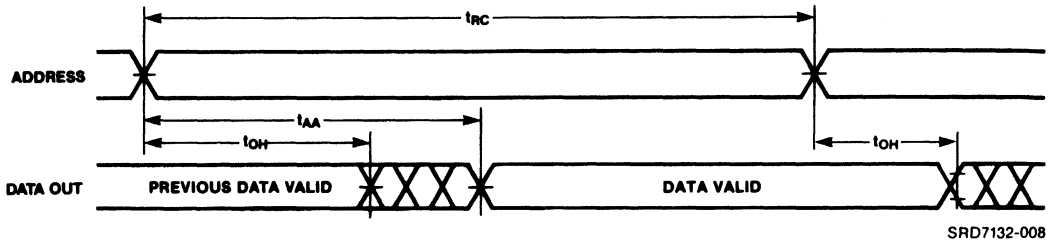
NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.

LOW V_{CC} DATA RETENTION WAVEFORM



SRD7132-016

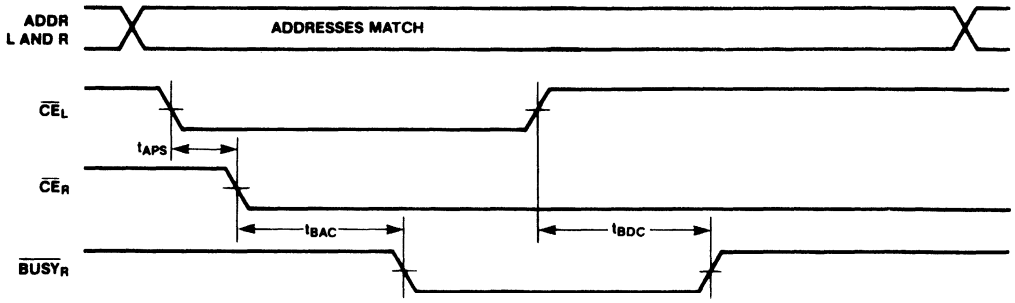
TIMING WAVEFORM OF READ CYCLE NO. 1 EITHER SIDE[1,2,6]



SRD7132-008

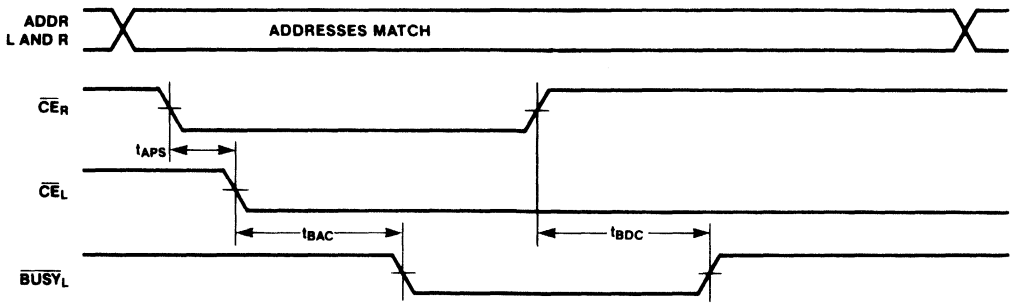
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1 $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:



SRD7132-012

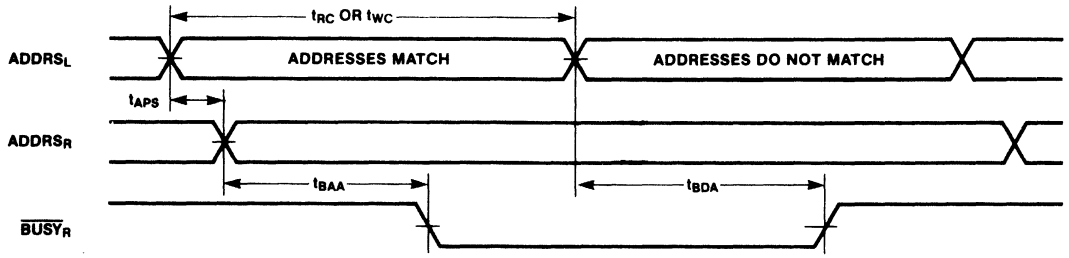
$\overline{CE}_R$ VALID FIRST:



SRD7132-013

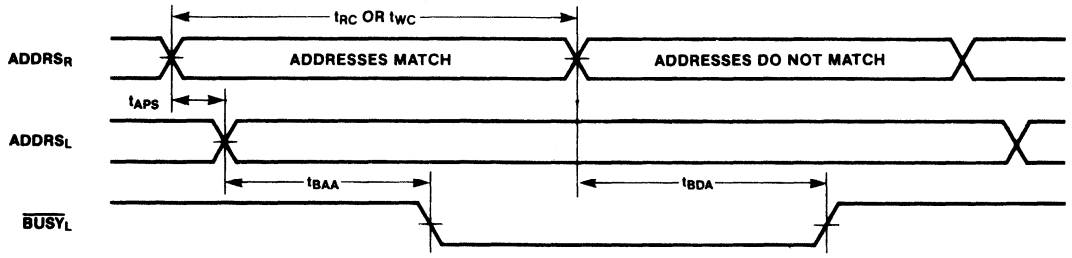
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2 ADDRESS VALID ARBITRATION(5)

LEFT ADDRESS VALID FIRST



SRD7132-014

RIGHT ADDRESS VALID FIRST

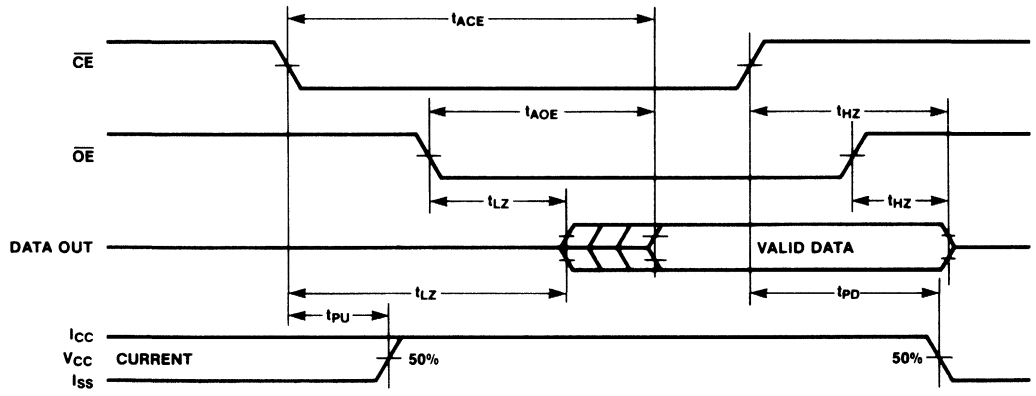


SRD7132-015

NOTES:

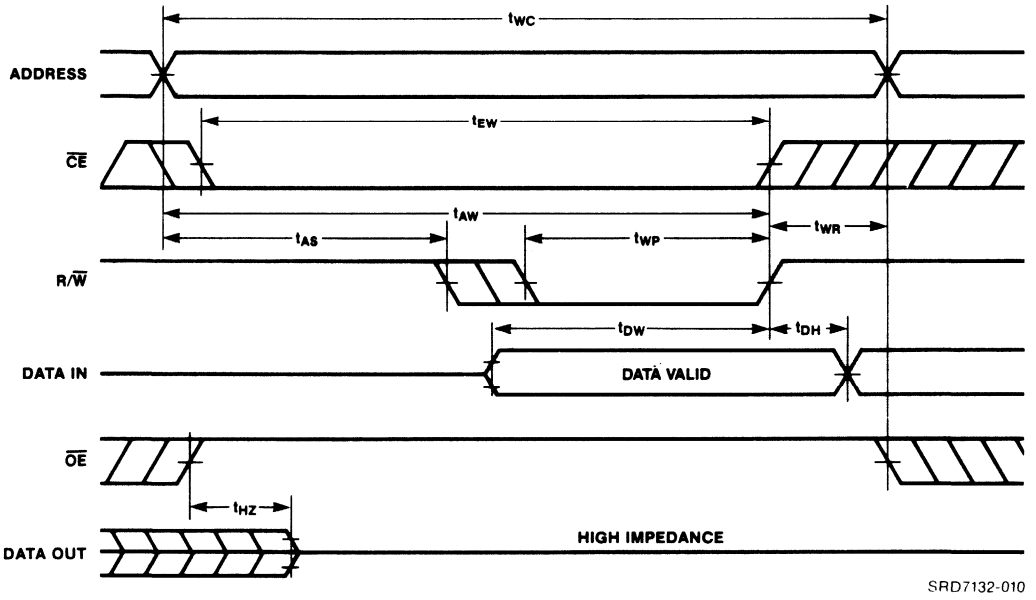
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. If $\overline{CE}$ goes high simultaneously with R/$\overline{W}$ high, the outputs remain in the high impedance state.
5. $\overline{CE}_L$ = $\overline{CE}_R$ = V_{IL}.
6. $\overline{OE}$ = V_{IL}.
7. R/$\overline{W}$ = V_{IH} during address transition.

TIMING WAVEFORM OF READ CYCLE NO. 2 EITHER SIDE[1,3]



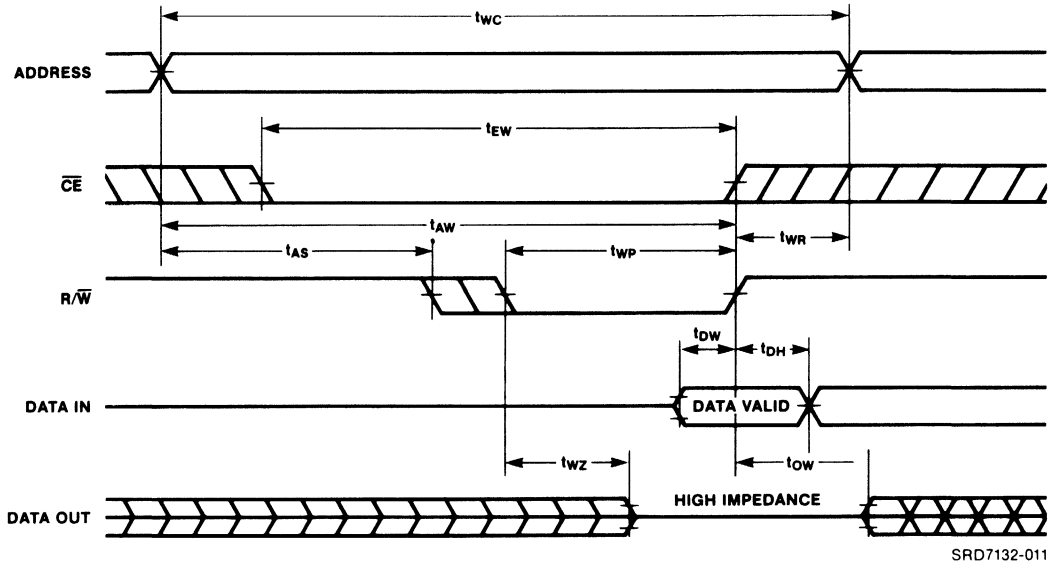
SRD7132-009

TIMING WAVEFORM OF WRITE CYCLE NO. 2 EITHER SIDE[4,7]



SRD7132-010

TIMING WAVEFORM OF WRITE CYCLE NO. 1 EITHER SIDE[4,7]



SRD7132-011

FUNCTIONAL DESCRIPTION:

The IDT7132 provides two ports with separate controls, address and I/O that permit independent access for reads or writes to any location in memory. The IDT7132 has an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access (refer to Table II, $\overline{CE}$ Arbitration); or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table III, Address Arbitration). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

TRUTH TABLES

TABLE I — NON-CONTENTION READ/WRITE CONTROL

LEFT PORT INPUTS[1]			RIGHT PORT INPUTS [1]			FLAGS		FUNCTION
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	H	X	X	X	X	H	H	Left Port in Power Down Mode
X	X	X	X	H	X	H	H	Right Port in Power Down Mode
L	L	X	X	X	X	H	H	Data on Left Port Written Into Memory
H	L	L	X	X	X	H	H	Data in Memory Output on Left Port
X	X	X	L	L	X	H	H	Data on Right Port Written Into Memory
X	X	X	H	L	L	H	H	Data in Memory Output on Right Port

NOTE:
1. A_{0L}-$A_{10L} \neq A_{0R}$-A_{10R}
H = HIGH, L = LOW, X = DON'T CARE

TABLE II — $\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$

LEFT PORT				RIGHT PORT				FLAGS		FUNCTION
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{10L}	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{10R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	LBR	X	MATCH	X	L	X	MATCH	H	L	Left Operation Permitted Right Operation Not Permitted
X	L	X	MATCH	X	LBL	X	MATCH	L	H	Left Operation Not Permitted Right Operation Permitted
X	LST	X	MATCH	X	LST	X	MATCH	H	L	Arbitration Resolved

NOTE:
X = DON'T CARE, L = LOW, H = HIGH, LST = Low Same Time, LBR = Low Before Right, LBL = Low Before Left

TABLE III — ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH

LEFT PORT				RIGHT PORT				FLAGS		FUNCTION
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{10L}	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{10R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	L	X	VBR	X	L	X	VALID	H	L	Left Operation Permitted Right Operation Not Permitted
X	L	X	VALID	X	L	X	VBL	L	H	Left Operation Not Permitted Right Operation Permitted
X	L	X	VST	X	L	X	VST	H	L	Arbitration Resolved

NOTE:
X = DON'T CARE, L = LOW, H = HIGH, VST = Valid Same Time, VBR = Valid Before Right, VBL = Valid Before Left

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, and 3

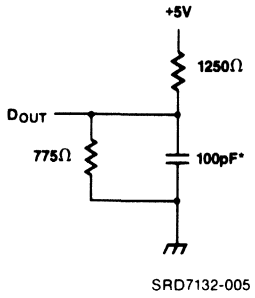


Figure 1.
Output Load

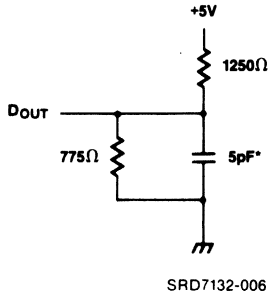


Figure 2.
Output Load
(for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

***Including scope and jig.**

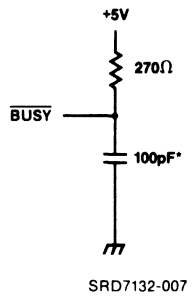


Figure 3.
$\overline{BUSY}$ Output Load

CAPACITANCE T_A = +25°C, f = 1.0 MHz

SYMBOL	TEST	CONDITIONS	TYP.	UNIT
C_{OUT}	Output Capacitance	V_{IN} = 0V	10	pF
C_{IN}	Input Capacitance	V_{OUT} = 0V	10	pF

NOTE:
This parameter is sampled and not 100% tested.

HIGH-SPEED CMOS DIGITAL SIGNAL PROCESSING PRODUCTS

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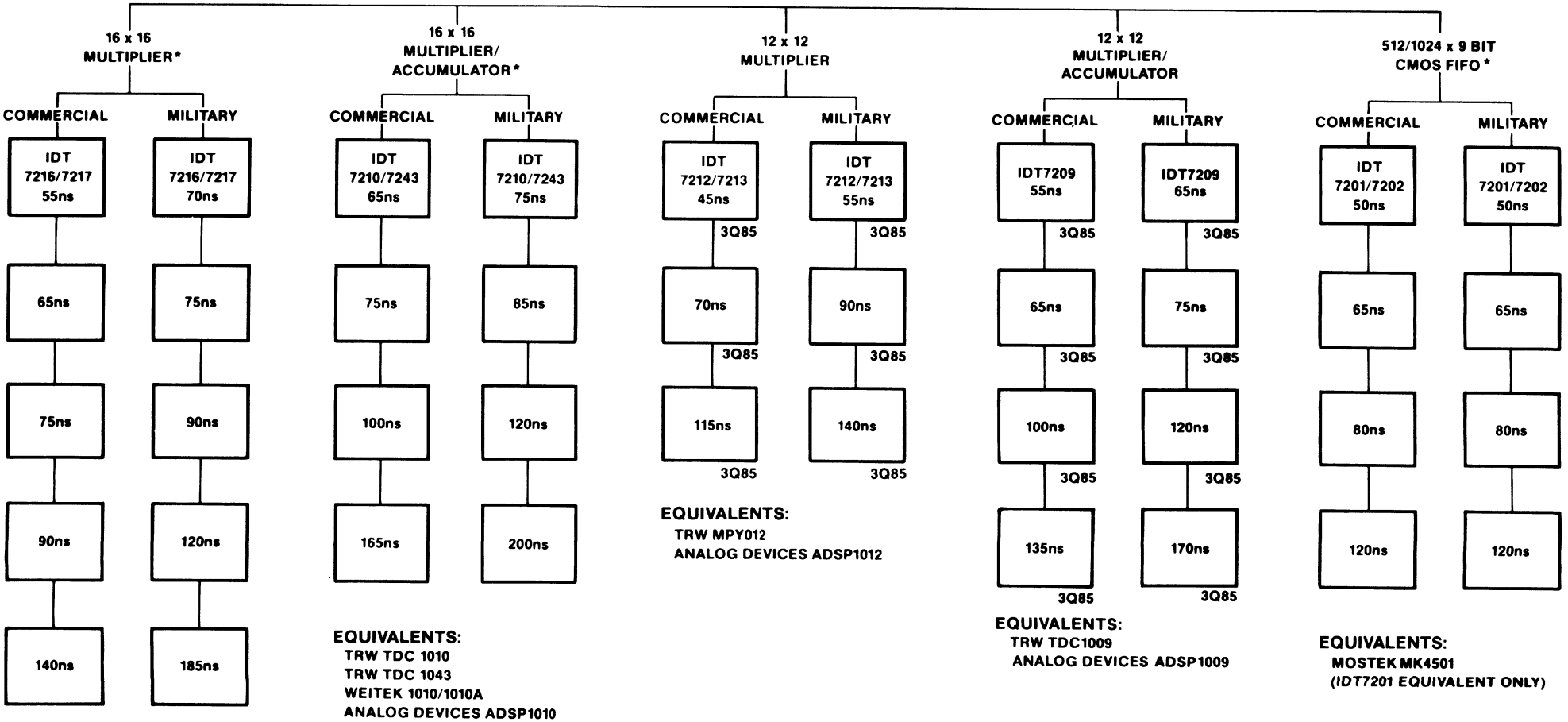
Integrated Device Technology, Inc.

LEADING THE CMOS FUTURE

DIGITAL SIGNAL PROCESSING DIVISION PRODUCT CROSS-REFERENCE GUIDE



*IN PRODUCTION NOW

Dates represent sample availability.

CEMOS is a trademark of Integrated Device Technology, Inc.

Speeds represent worst case, not typical values.

Integrated Device Technology, Inc.

16x16 BIT PARALLEL CMOS MULTIPLIER

IDT7216L
IDT7217L

DSP

FEATURES:

- 16x16 parallel multiplier with double precision product
- High-speed 55ns maximum clock to multiply time
- Low power consumption - 200mW typical, less than 1/10th the power of compatible bipolar parts
- Produced with advanced CEMOS™ I high-performance technology
- IDT7216L is pin and functionally compatible with TRW MPY016H/K and AMD AM29516
- IDT7217L requires only single clock with register enables making it pin and functionally compatible with AMD AM29517
- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round control for rounding the MSP
- Single 5V power supply
- Input and output directly TTL-compatible
- Three-state output
- Available in DIP, LCC or Flatpack
- Military product available 100% screened to Class B

DESCRIPTION:

The IDT7216/IDT7217 are high-speed, low-power 16x16 multipliers, ideal for fast, real time digital signal processing applications. Utilization of a modified Booths algorithm and IDT's high-performance, high-reliability technology, CEMOS I, has achieved speeds comparable to bipolar (55ns max.) at 1/10th the power consumption.

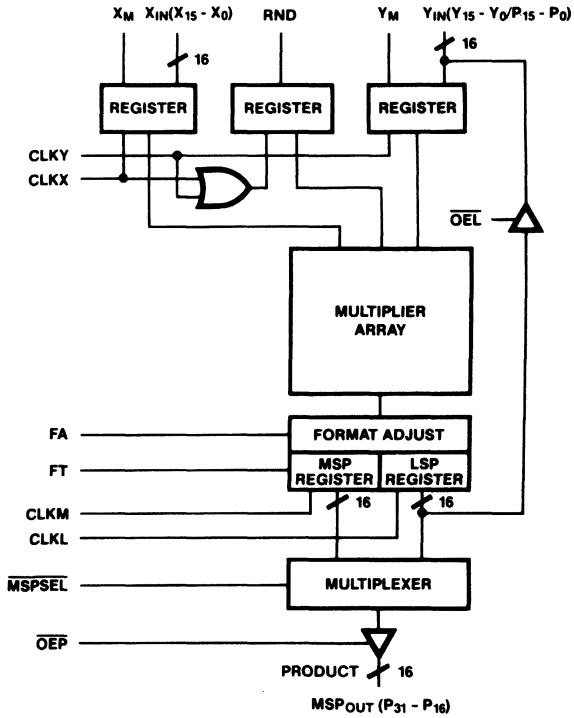
The IDT7216/IDT7217 are ideal for applications requiring high-speed multiplications such as fast Fourier transform analysis, digital filtering, graphic display systems, speech synthesis and recognition, and in any system requirement where multiplication speeds of a mini/micro computer are inadequate.

All input registers, as well as LSP and MSP output registers, use the same positive edge triggered D-type flip-flop. In the IDT7216, there are independent clocks (CLKX, CLKY, CLKM, CLKL) associated with each of these registers. The IDT7217 has only a single clock input (CLK) and three register enables. $\overline{ENX}$ and $\overline{ENY}$ control the two input registers, while $\overline{ENP}$ controls the entire product.

The IDT7216/IDT7217 offer additional flexibility with the FA control and $\overline{MSPSEL}$ functions. The FA control formats the output for 2's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP. The $\overline{MSPSEL}$ low selects the MSP to be available at the product output port, while a high selects the LSP to be available. Keeping this pin low will ensure compatibility with the TRW MPY016H/K.

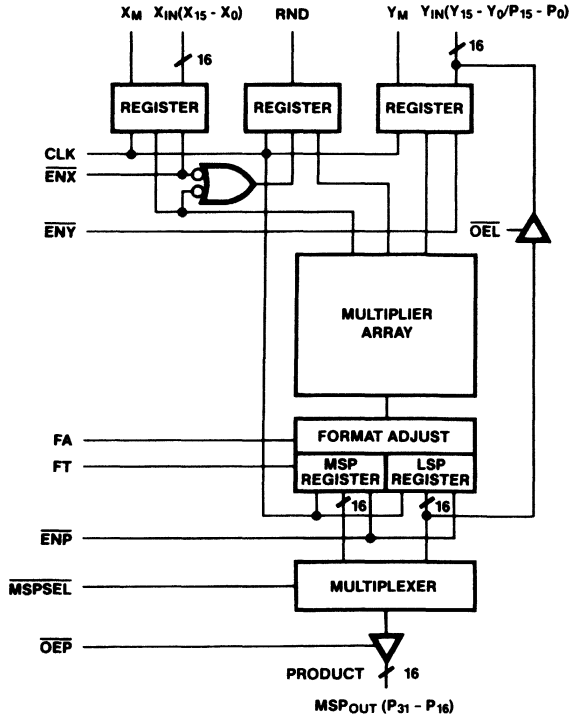
The IDT7216/IDT7217 Multipliers are 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAMS



IDT7216

DSP7216-001



IDT7217

DSP7216-002

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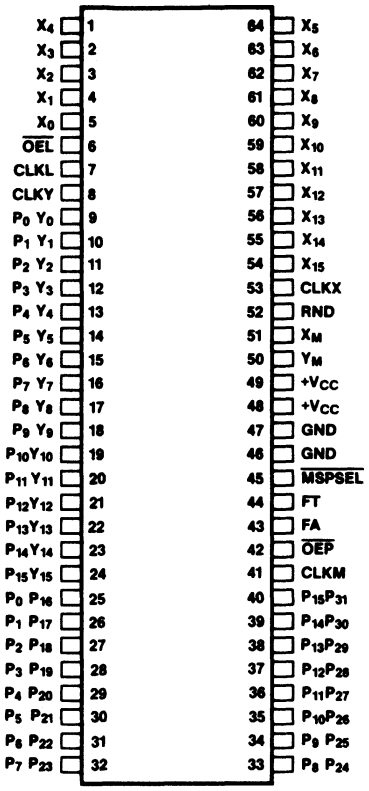
MILITARY AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

PIN CONFIGURATIONS

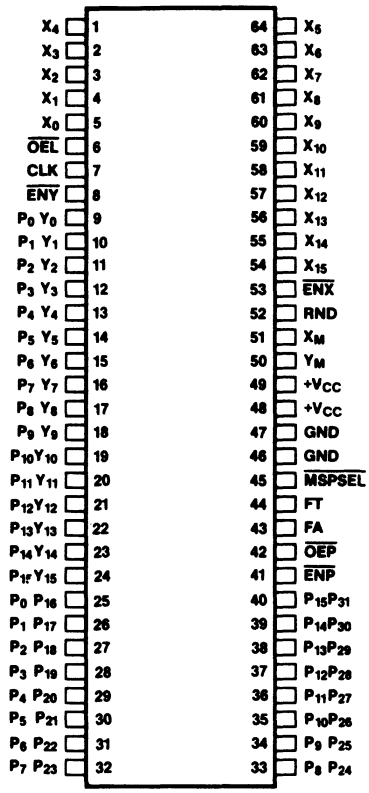
IDT7216 CMOS MULTIPLIER
64-PIN DIP



DSP7216-003

TOP VIEW

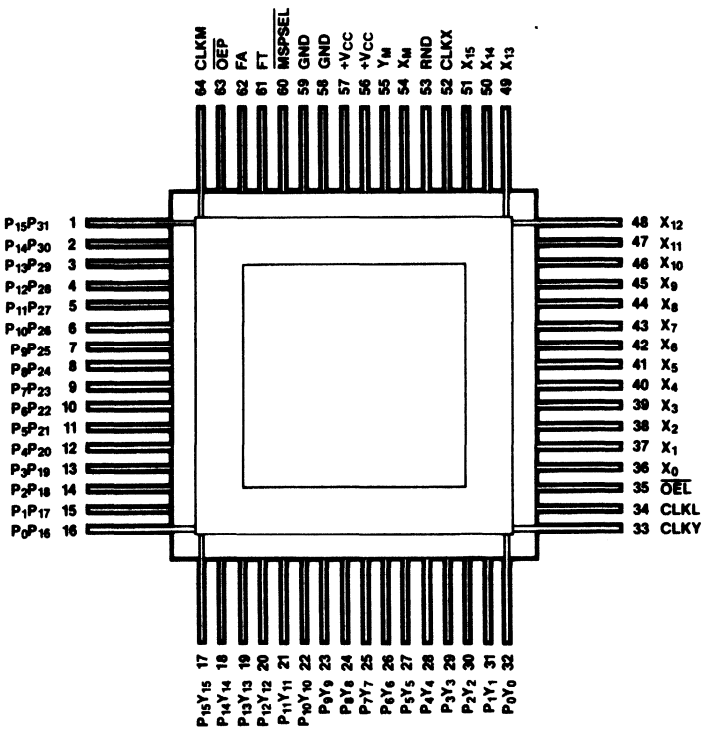
IDT7217 CMOS MULTIPLIER
64-PIN DIP



DSP7216-004

TOP VIEW

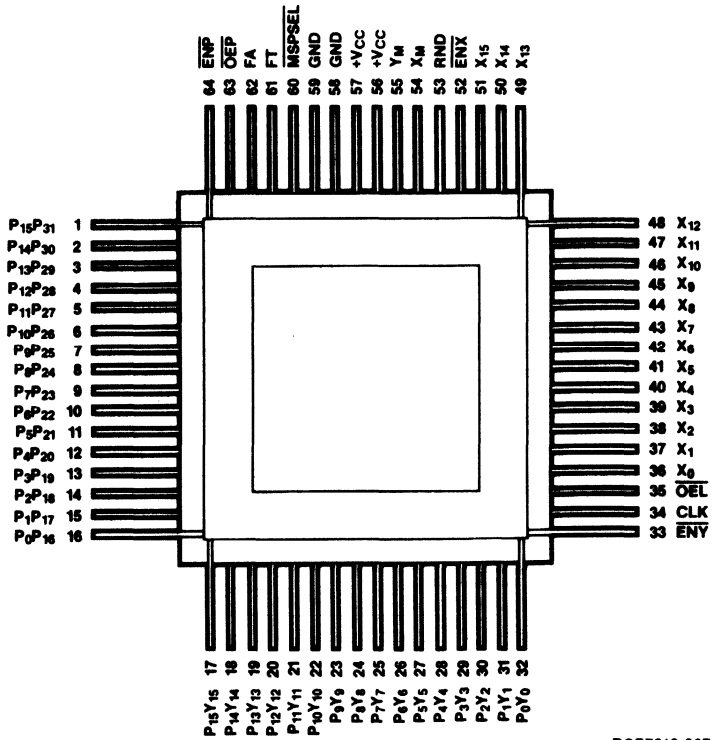
IDT7216 CMOS MULTIPLIER 64-LEAD FLATPACK



DSP7216-005

TOP VIEW

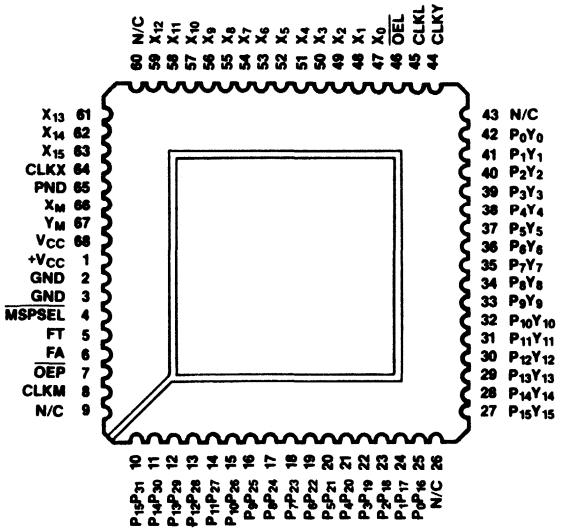
IDT7217 CMOS MULTIPLIER 64-LEAD FLATPACK



DSP7216-007

TOP VIEW

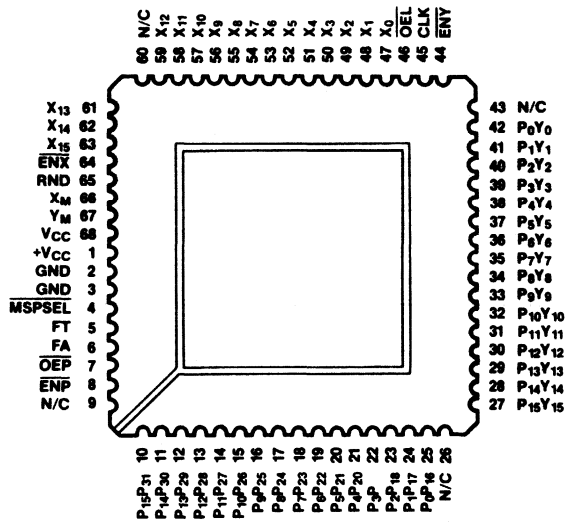
IDT7216 CMOS MULTIPLIER 68-PIN LCC



DSP7216-006

TOP VIEW

IDT7217 CMOS MULTIPLIER 68-PIN LCC



DSP7216-008

TOP VIEW

DSP

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}	Input Low Voltage	—	—	0.8	V

DC ELECTRICAL CHARACTERISTICS (Commercial: V_{CC} = 5V ± 5%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	TEST CONDITIONS	TMC = 55, 65ns COMMERCIAL MIN.	TYP.[1]	MAX.	TMC = 70, 75ns MILITARY MIN.	TYP.[1]	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max, V_{IN} = 0 to V_{CC}	—	—	75	—	—	100	µA
$\|I_{LO}\|$	Output Leakage Current	High Z, V_{CC} = max., V_{OUT} = 0 to V_{CC}	—	—	75	—	—	100	µA
I_{CC}[2]	Operating Power Supply Current	Output Open	—	40	80	—	40	100	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	50	—	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ – .2V or ≤ .2V	—	4	20	—	4	25	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –0.4mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0mA	—	—	0.5	—	—	0.5	V

SYMBOL	PARAMETER	TEST CONDITIONS	TMC = 75, 90, 140ns COMMERCIAL MIN.	TYP.[1]	MAX.	TMC = 90, 120, 185ns MILITARY MIN.	TYP.[1]	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max, V_{IN} = 0 to V_{CC}	—	—	2	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	High Z, V_{CC} = max., V_{OUT} = 0 to V_{CC}	—	—	2	—	—	10	µA
I_{CC}[2]	Operating Power Supply Current	Output Open	—	30	60	—	30	80	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	10	30	—	10	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ – .2V or ≤ .2V	—	0.1	1.0	—	0.1	2.0	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –0.4mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0mA	—	—	0.5	—	—	0.5	V

NOTES:
1. V_{CC} = 5V, T_A = +25°C.
2. I_{CC} is measured at clock cycle = 10MHz and V_{IN} = TTL voltages.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
This parameter is sampled and not 100% tested.

AC TEST CONDITONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

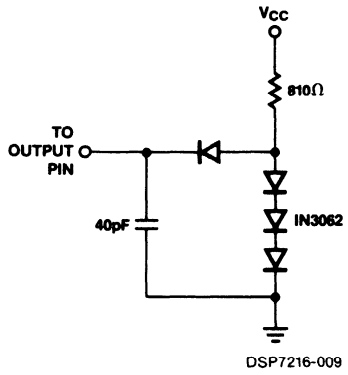


Figure 1. AC Output Test Load

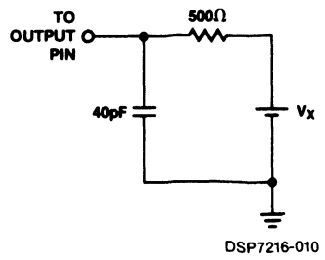


Figure 2. Output Three State Delay Load (V_X = 0V or 2.6V)

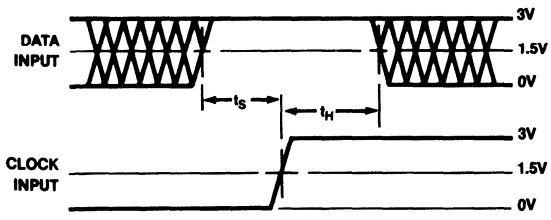
AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ± 5%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7216L-55 IDT7217L-55 MIN.	MAX.	IDT7216L-65 IDT7217L-65 MIN.	MAX.	IDT7216L-75 IDT7217L-75 MIN.	MAX.	IDT7216L-90 IDT7217L-90 MIN.	MAX.	IDT7216L-140 IDT7217L-140 MIN.	MAX.	UNIT	TEST LOAD FIG.
t_{MUC}	Unclocked Multiply Time	—	75	—	85	—	110	—	125	—	180	ns	1
t_{MC}	Clocked Multiply Time	—	55	—	65	—	75	—	90	—	140	ns	1
t_S	X, Y, RND Setup Time	20	—	20	—	25	—	25	—	25	—	ns	1
t_H	X, Y, RND Hold Time	3	—	3	—	2	—	0	—	0	—	ns	1
t_{PWH}	Clock Pulse Width High	15	—	15	—	20	—	20	—	25	—	ns	1
t_{PWL}	Clock Pulse Width Low	20	—	20	—	20	—	20	—	25	—	ns	1
t_{PDSEL}	$\overline{\text{MSPSEL}}$ to Product Out	—	30	—	30	—	35	—	35	—	40	ns	1
t_{PDP}	Output Clock to P	—	30	—	30	—	35	—	35	—	40	ns	1
t_{PDY}	Output Clock to Y	—	30	—	30	—	35	—	35	—	40	ns	1
t_{ENA}	3 State Enable Time[2]	—	30	—	35	—	35	—	35	—	40	ns	2
t_{DIS}	3 State Disable Time[2]	—	20	—	20	—	30	—	30	—	40	ns	2
t_S	Clock Enable Setup Time (IDT7217 only)	10	—	10	—	25	—	25	—	25	—	ns	1
t_H	Clock Enable Hold Time (IDT7217 only)	3	—	3	—	3	—	3	—	3	—	ns	1
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML[1] (IDT7216 only)	0	—	0	—	0	—	0	—	0	—	ns	1

AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7216L-70 IDT7217L-70 MIN.	MAX.	IDT7216L-75 IDT7217L-75 MIN.	MAX.	IDT7216L-90 IDT7217L-90 MIN.	MAX.	IDT7216L-120 IDT7217L-120 MIN.	MAX.	IDT7216L-185 IDT7217L-185 MIN.	MAX.	UNIT	TEST LOAD FIG.
t_{MUC}	Unclocked Multiply Time	—	85	—	95	—	130	—	160	—	230	ns	1
t_{MC}	Clocked Multiply Time	—	70	—	75	—	90	—	120	—	185	ns	1
t_S	X, Y, RND Setup Time	25	—	25	—	30	—	30	—	30	—	ns	1
t_H	X, Y, RND Hold Time	3	—	3	—	2	—	0	—	0	—	ns	1
t_{PWH}	Clock Pulse Width High	15	—	15	—	30	—	30	—	30	—	ns	1
t_{PWL}	Clock Pulse Width Low	15	—	15	—	30	—	30	—	30	—	ns	1
t_{PDSEL}	$\overline{\text{MSPSEL}}$ to Product Out	—	35	—	35	—	40	—	40	—	45	ns	1
t_{PDP}	Output Clock to P	—	35	—	35	—	40	—	40	—	45	ns	1
t_{PDY}	Output Clock to Y	—	35	—	35	—	40	—	40	—	45	ns	1
t_{ENA}	3 State Enable Time[2]	—	35	—	40	—	40	—	40	—	45	ns	2
t_{DIS}	3 State Disable Time[2]	—	22	—	22	—	40	—	40	—	45	ns	2
t_S	Clock Enable Setup Time (IDT7217 only)	15	—	15	—	30	—	30	—	30	—	ns	1
t_H	Clock Enable Hold Time (IDT7217 only)	3	—	3	—	3	—	3	—	3	—	ns	1
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML[1] (IDT7216 only)	0	—	0	—	0	—	0	—			ns	1

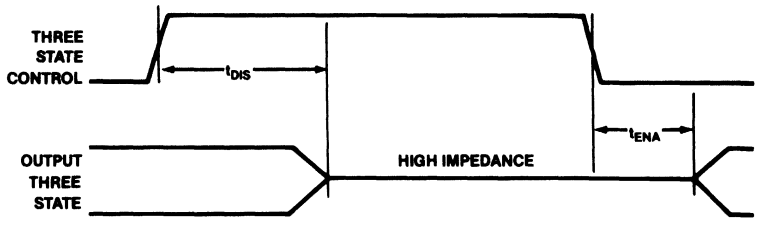
NOTES:
1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured ±500mV from steady state voltage with loading specified in Fig. 2.



NOTE:
Diagram shown for HIGH data only. Output transition may be opposite sense.

DSP7216-011

Figure 3. Set-Up And Hold Time



DSP7216-012

Figure 4. Three-State Control Timing Diagram

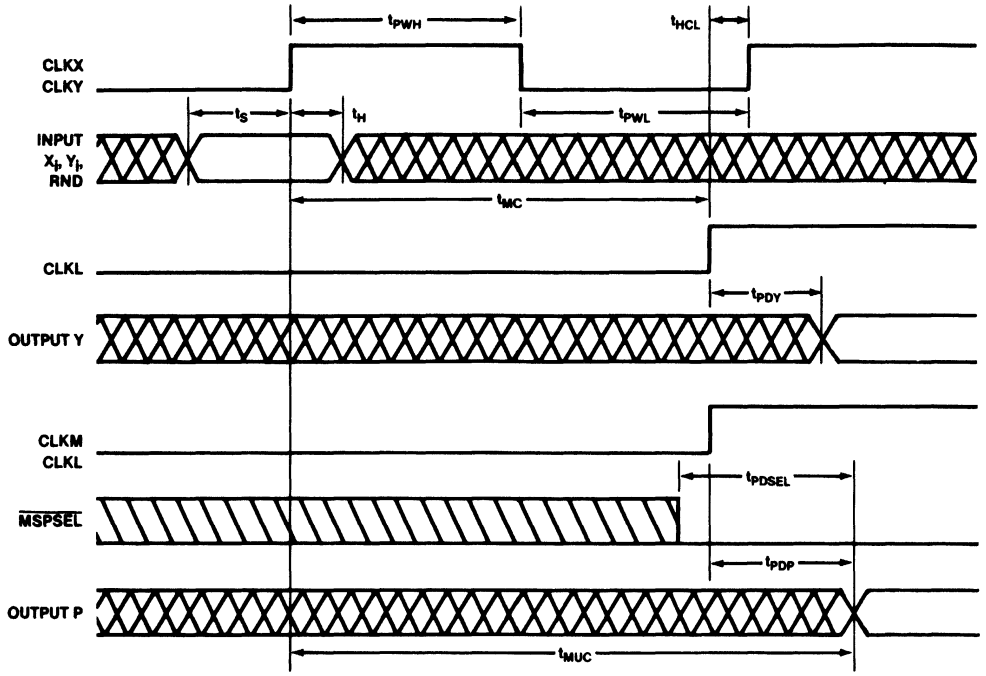


Figure 5. IDT7216 Timing Diagram

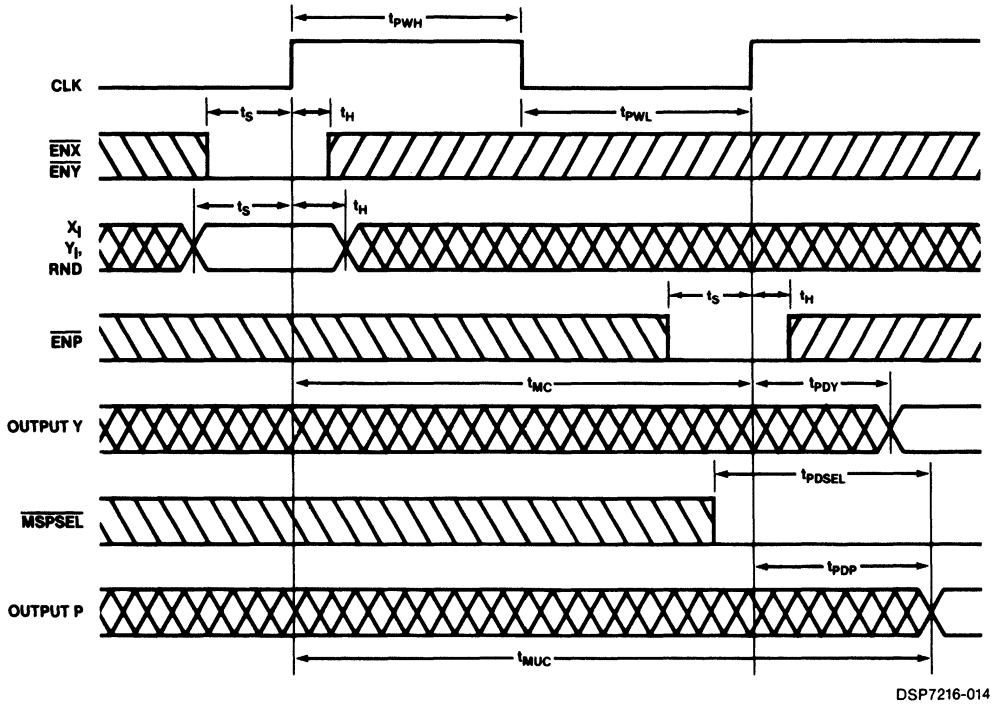
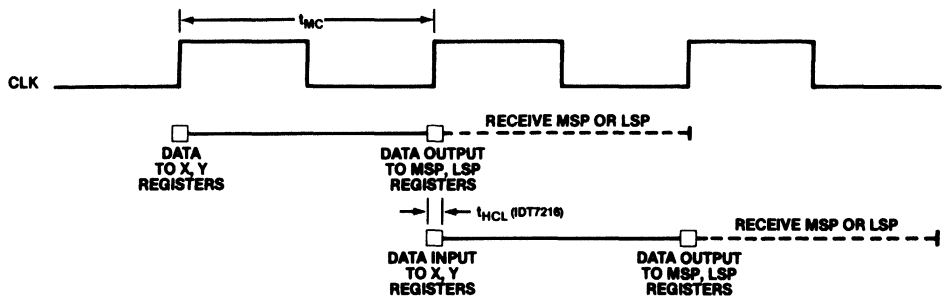


Figure 6. IDT7217 Timing Diagram



DSP7216-015

Figure 7. Simplified Timing Diagram - Typical Application

SIGNAL DESCRIPTIONS:

INPUTS:

X_{IN} (X_{15} through X_0)
Sixteen Multiplicand Data Inputs

Y_{IN} (Y_{15} through Y_0)
Sixteen Multiplier Data Inputs

INPUT CLOCKS (IDT7216 ONLY):

CLKX
The rising edge of this clock loads the X_{15} - X_0 data input register along with the two's complement and round registers.

CLKY
The rising edge of this clock loads the Y_{15} - Y_0 data input register along with the two's complement and round registers.

CLKM
The rising edge of this clock loads the Most Significant Product (MSP) register.

CLKL
The rising edge of this clock loads the Least Significant Product (LSP) register.

INPUT CLOCKS (IDT7217 ONLY):

CLK
The rising edge of this clock loads all registers.

$\overline{ENX}$
Register enable for the X_{15} - X_0 data input register along with the two's complement and round registers.

$\overline{ENY}$
Register enable for the Y_{15} - Y_0 data input register along with the two's complement and round registers.

$\overline{ENP}$
Register enable for the Most Significant Product (MSP) and Least Significant Product (LSP).

CONTROLS:

Xm, Ym (TCX, TCY)[1]
Mode control inputs for each data word. A low input in designates unsigned data input with a high input used for two's complement.

FA (RS)[1]
When the format adjust control is HIGH, a full 32-bit product is selected. When this control is LOW, a left-shifted 31-bit product is selected with the sign bit replicated in the Least Significant Product (LSP). This control is normally HIGH except for certain fractional two's complement applications. (See Multiplier Input/Output Formats.)

FT
When this control is HIGH, both the Most Significant Product (MSP) and Least Significant Product (LSP) registers are transparent.

$\overline{OEL}$
Three-state enable for routing LSP through Y_{IN}/LSP_{OUT} port.

$\overline{OEP}$
Three-state enable for the product output port.

RND
Round control for the rounding of the Most Significant Product (MSP). When this control is HIGH, a one is added to the Most Significant Bit (MSB) of the Least Significant Product (LSP). Note that this bit depends on the state of the format adjust (FA) control. If FA is LOW when RND is HIGH, a one will be added to the 2^{-16}-bit (P_{14}). If FA is HIGH when RND is HIGH, a one will be added to the 2^{-15}-bit (P_{15}). In either case, the LSP output will reflect this addition when RND is HIGH. Note also that rounding always occurs in the positive direction which may introduce a systematic bias. The RND input is registered and clocked in at the rising edge of the logical OR of both CLKX and CLKY.

$\overline{MSPSEL}$
When the $\overline{MSPSEL}$ is LOW, the Most Significant Product (MSP) is selected. When HIGH, the Least Significant Product (LSP) is available at the product output port.

OUTPUTS:

MSP (P_{31} through P_{16})
Most Significant Product Output

LSP (P_{15} through P_0)
Least Significant Product Output

Y_{IN}/LSP_{OUT} (Y_{15} through Y_0 or P_{15} through P_0)
Least Significant Product (LSP) Output available when $\overline{OEL}$ is LOW.

NOTE:
1. TRW MPY016H/K pin designation.

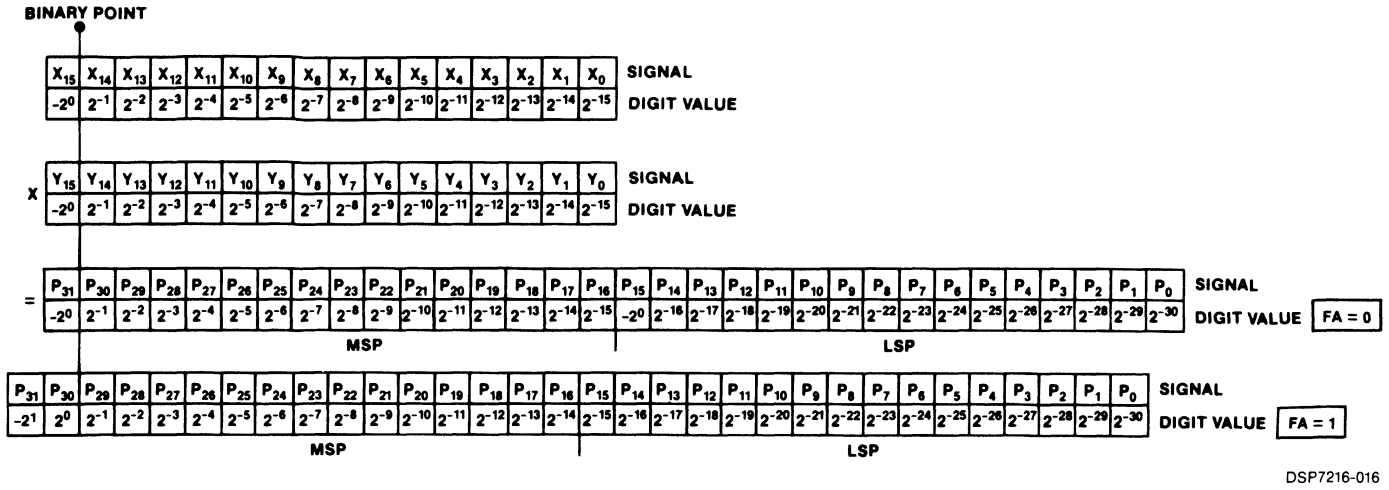


Figure 8. Fractional Two's Complement Notation

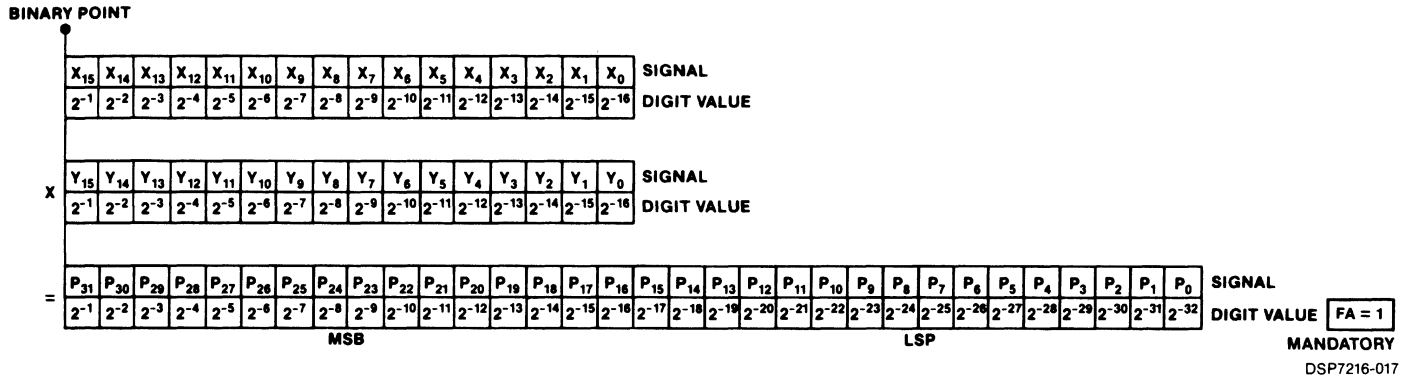


Figure 9. Fractional Unsigned Magnitude Notation

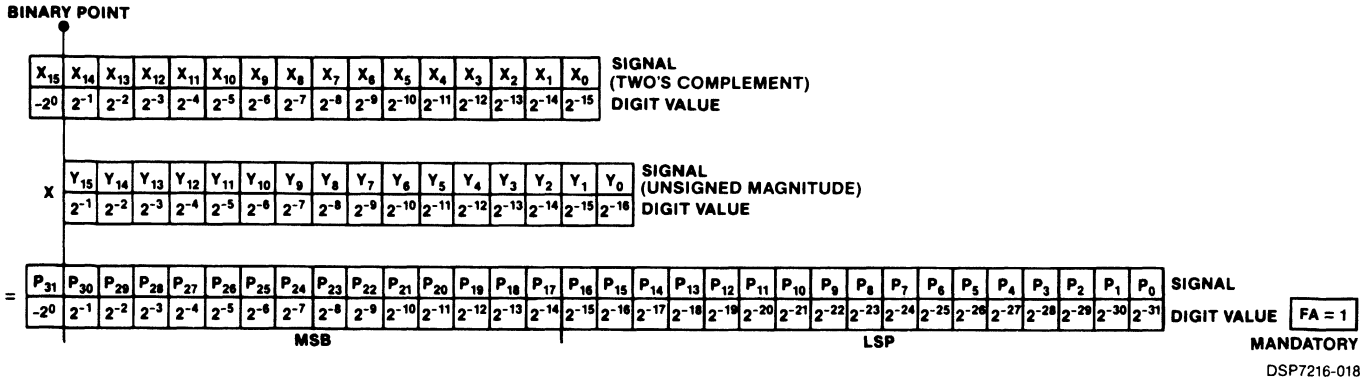


Figure 10. Fractional Mixed Mode Notation

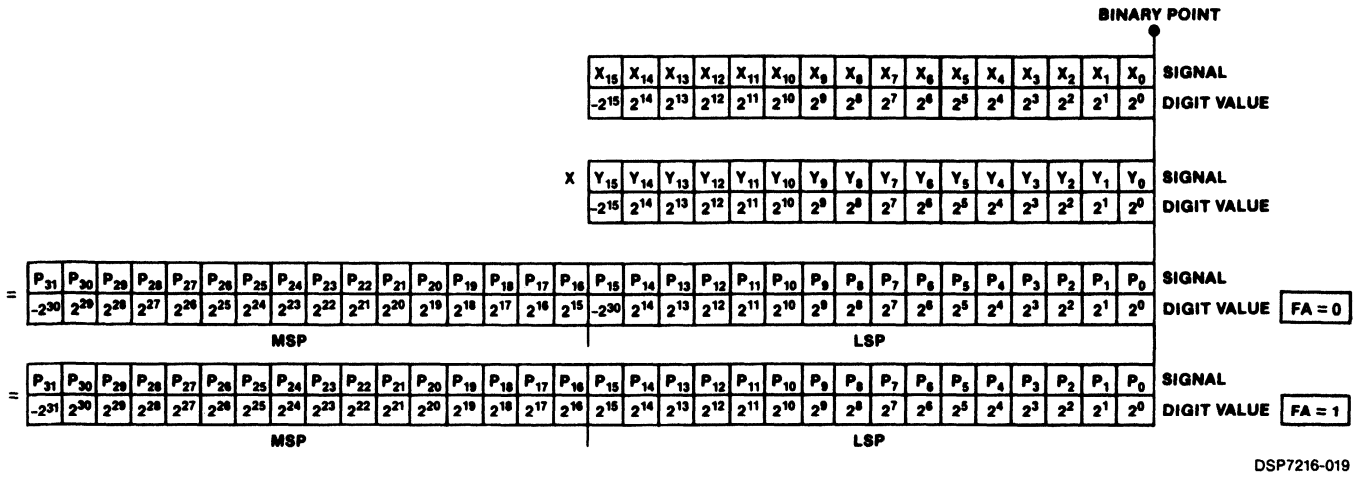


Figure 11. Integer Two's Complement Notation

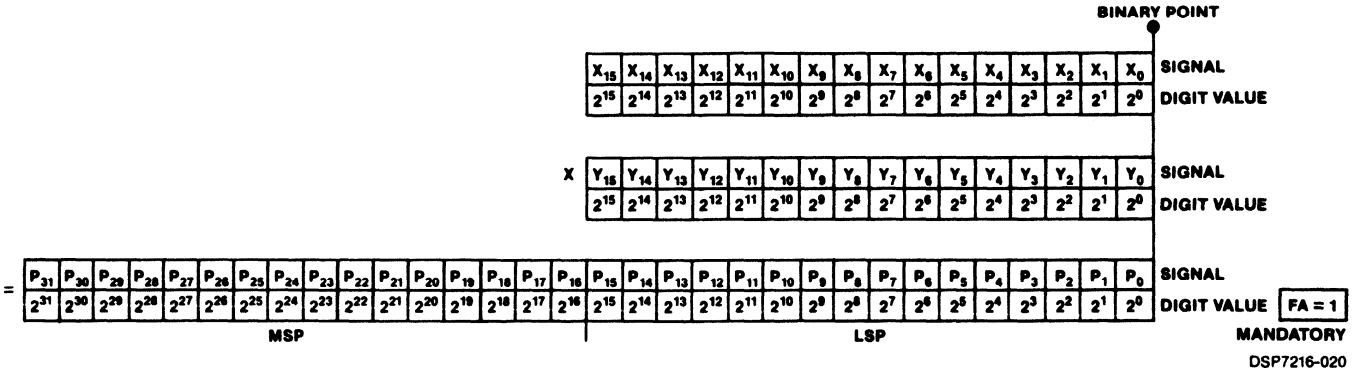


Figure 12. Integer Unsigned Magnitude Notation

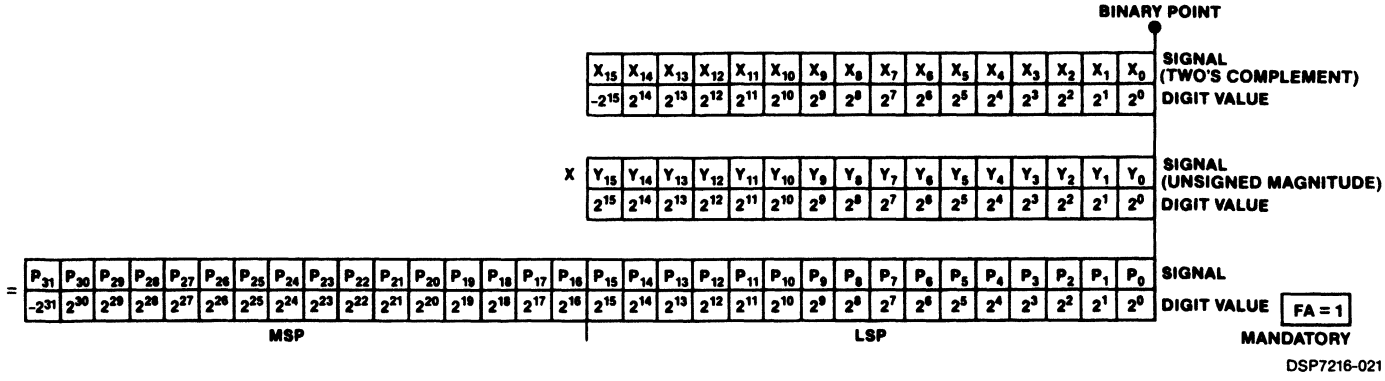


Figure 13. Integer Mixed Mode Notation

Integrated Device Technology, Inc.

12 x 12 BIT PARALLEL CMOS MULTIPLIER

PRELIMINARY
IDT7212
IDT7213

FEATURES:

- 12x12 parallel multiplier with double precision product
- High-speed - 45ns maximum clock to multiply time
- Low power consumption - 250mW typical, less than 1/10th the power of compatible bipolar parts
- Produced with advanced sub-2 micron CEMOS™ II dual-layer metal high-performance technology
- IDT7212L is pin and functionally compatible with TRW MPY012H
- IDT7213L requires only a single clock with register enables
- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round control for rounding the MSP
- Single 5V power supply
- Input and output directly TTL-compatible
- Three-state output
- Available in DIP, LCC or Flatpack
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7212/IDT7213 are high-speed, low power 12x12 multipliers ideal for fast, real-time digital signal processing applications. Utilization of a modified Booths algorithm and IDT's high-performance, high-reliability technology, CEMOS II, has achieved speeds exceeding bipolar (45ns max.) at 1/10th the power consumption.

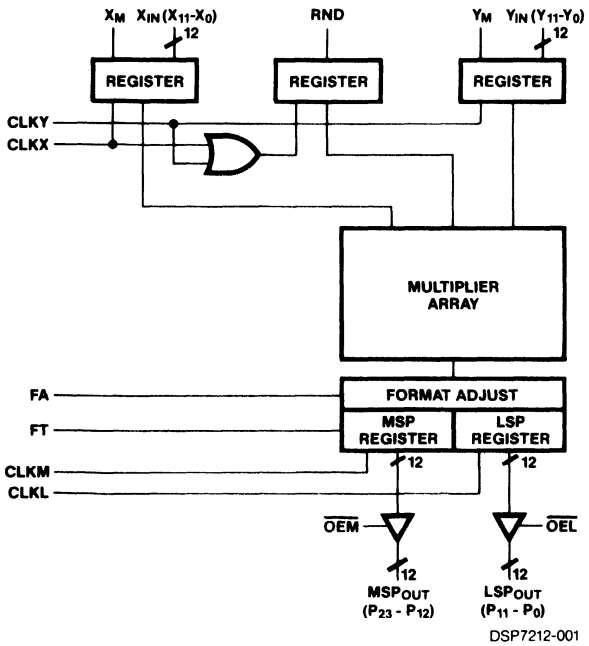
The IDT7212/IDT7213 are ideal for applications requiring high-speed multiplications such as fast Fourier transform analysis, digital filtering, graphic display systems, speech synthesis and recognition, and in any system requirement where multiplication speeds of a mini/micro computer are inadequate.

All input registers, as well as LSP and MSP output registers, use the same positive edge triggered D-type flip-flop. With the IDT7212, there are independent clocks (CLKX, CLKY, CLKM, CLKL) associated with each of these registers. The IDT7213 has only a single clock input (CLK) and three register enables. $\overline{ENX}$ and $\overline{ENY}$ control the two input registers, while $\overline{ENP}$ controls the entire product.

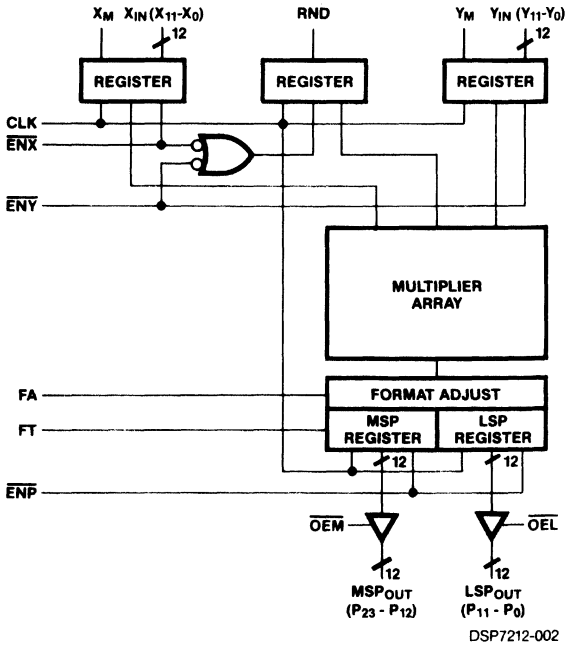
The IDT7212/IDT7213 offer additional flexibility with the FA control. The FA control formats the output for 2's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP.

The IDT7212/IDT7213 Multipliers are 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAMS



IDT7212



IDT7213

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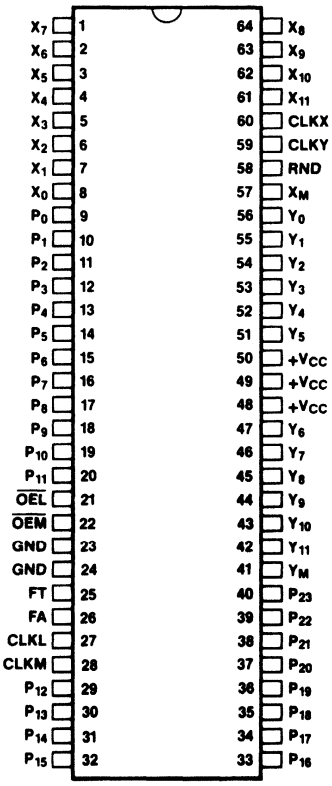
MILITARY AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

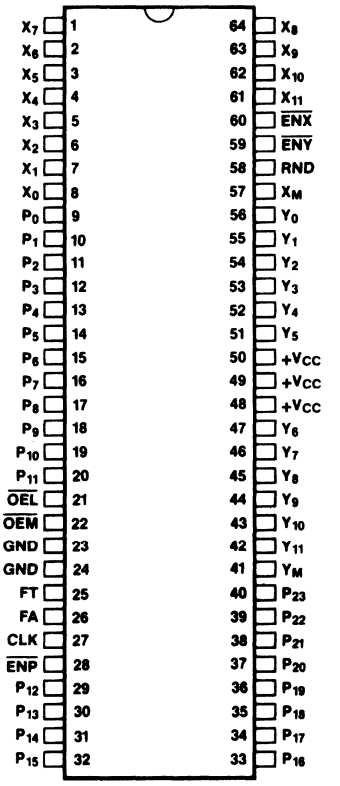
PIN CONFIGURATIONS

IDT7212 MULTIPLIER
64-PIN DIP



TOP VIEW DSP7212-003

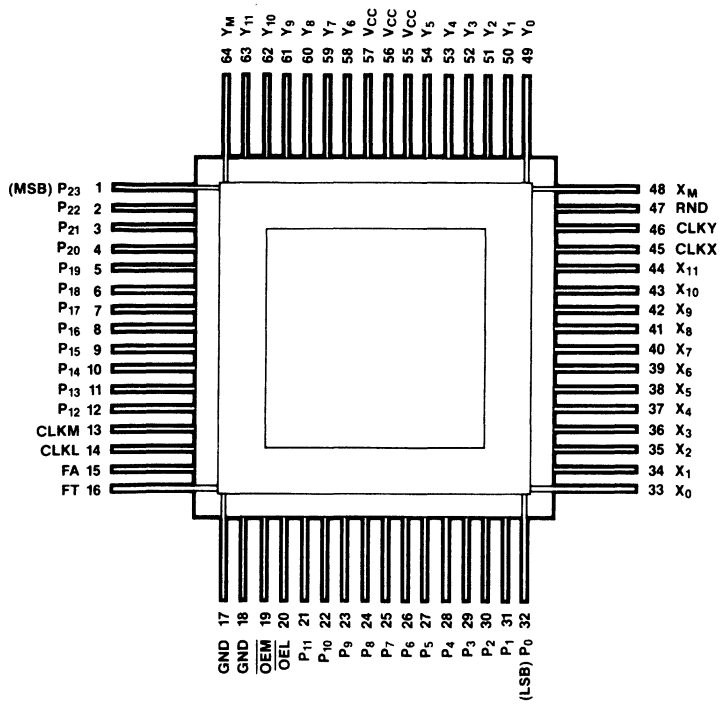
IDT7213 MULTIPLIER
64-PIN DIP



TOP VIEW DSP7212-004

DSP

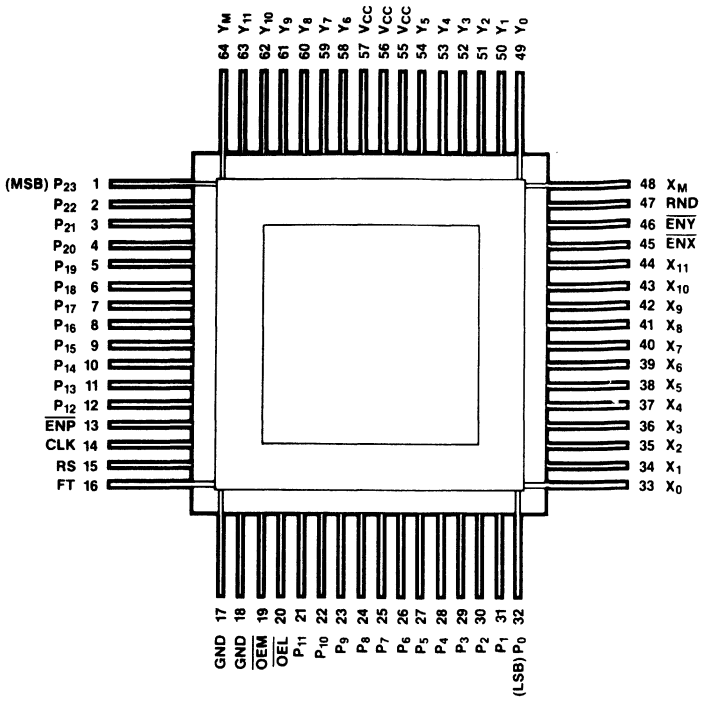
IDT7212 MULTIPLIER
64-LEAD FLATPACK



DSP7212-005

TOP VIEW

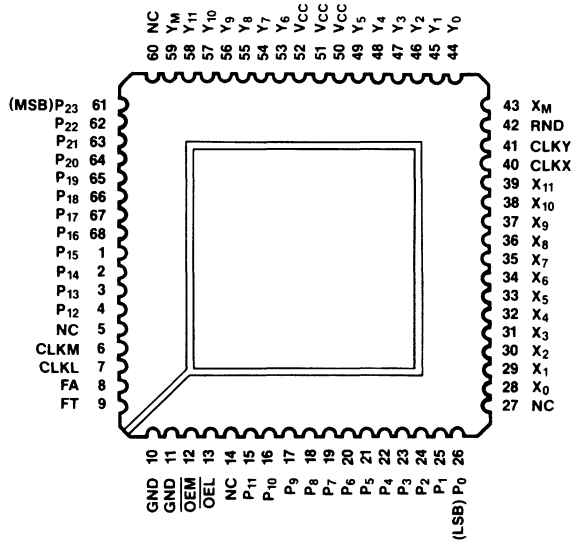
IDT7213 MULTIPLIER
64-LEAD FLATPACK



DSP7212-007

TOP VIEW

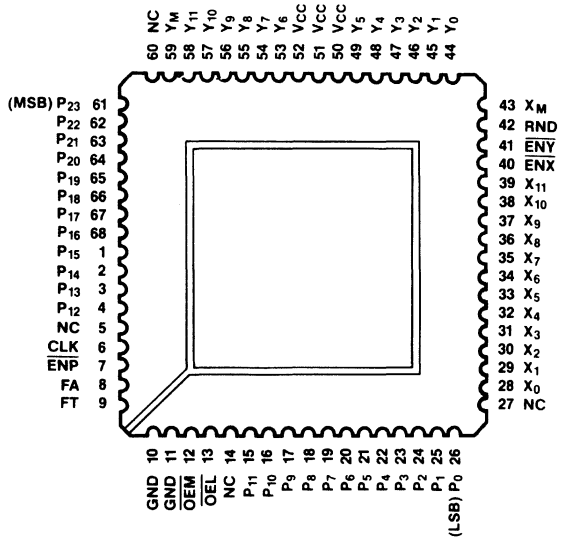
IDT7212 MULTIPLIER
68-PIN LCC



DSP7212-006

TOP VIEW

IDT7213 MULTIPLIER
68-PIN LCC



DSP7212-008

TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}	Input Low Voltage	—	—	0.8	V

DSP

DC ELECTRICAL CHARACTERISTICS (Commercial: V_{CC} = 5V ± 5%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	TEST CONDITIONS	TMC = 45, 70ns COMMERCIAL MIN	TYP[1]	MAX	TMC = 55, 90ns MILITARY MIN	TYP[1]	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	75	—	—	100	µA
I_{LO}	Output Leakage Current	High Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	—	—	75	—	—	100	µA
I_{CC}[2]	Operating Power Supply Current	Output Open	—	40	80	—	40	100	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	50	—	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ – .2V or ≤ .2V	—	4	20	—	4	25	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –0.4mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0mA	—	—	0.5	—	—	0.5	V

SYMBOL	PARAMETER	TEST CONDITIONS	TMC = 115ns COMMERCIAL MIN	TYP[1]	MAX	TMC = 140ns MILITARY MIN	TYP[1]	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	2	—	—	10	µA
I_{LO}	Output Leakage Current	High Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	—	—	2	—	—	10	µA
I_{CC}[2]	Operating Power Supply Current	Output Open	—	30	60	—	30	80	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	10	30	—	10	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ – .2V or ≤ .2V	—	0.1	1.0	—	0.1	2.0	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –0.4mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0mA	—	—	0.5	—	—	0.5	V

NOTES:
1. V_{CC} = 5V, T_A = +25°C.
2. I_{CC} is measured at clock cycle = 10MHz and V_{IN} = TTL voltages.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
This parameter is sampled and not 100% tested.

AC TEST CONDITONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

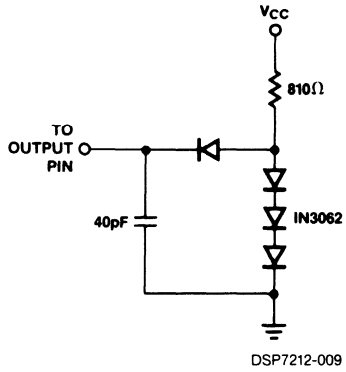


Figure 1. AC Output Test Load

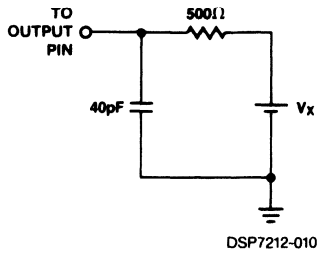


Figure 2. Output Three State Delay Load (V_X = 0V or 2.6V)

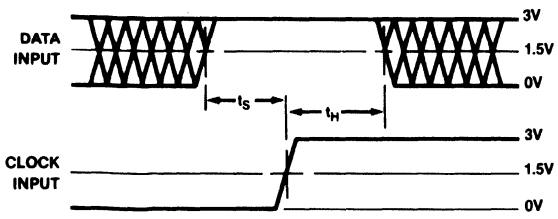
AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ± 5%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7212L45 IDT7213L45 MIN.	MAX.	IDT7212L70 IDT7213L70 MIN.	MAX.	IDT7212L115 IDT7213L115 MIN.	MAX.	UNIT	TEST LOAD FIG.
t_{MUC}	Unclocked Multiply Time	—	75	—	105	—	155	ns	1
t_{MC}	Clocked Multiply Time	—	45	—	70	—	115	ns	1
t_S	X, Y, RND Set-Up Time	20	—	25	—	25	—	ns	1
t_H	X, Y, RND Hold Time	3	—	2	—	0	—	ns	1
t_{PWH}	Clock Pulse Width High	20	—	20	—	25	—	ns	1
t_{PWL}	Clock Pulse Width Low	20	—	20	—	25	—	ns	1
t_{PDP}	Output Clock to P	—	35	—	35	—	40	ns	1
t_{ENA}	3 State Enable Time(2)	—	35	—	35	—	40	ns	2
t_{DIS}	3 State Disable Time(2)	—	35	—	35	—	40	ns	2
t_S	Clock Enable Setput Time (IDT7213 only)	25	—	25	—	25	—	ns	1
t_H	Clock Enable Hold Time (IDT7213 only)	3	—	3	—	0	—	ns	1
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML(1) (IDT7212 only)	0	—	0	—	0	—	ns	1

AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7212L55 IDT7213L55 MIN.	MAX.	IDT7212L90 IDT7213L90 MIN.	MAX.	IDT7212L140 IDT7213L140 MIN.	MAX.	UNIT	TEST LOAD FIG.
t_{MUC}	Unclocked Multiply Time	—	90	—	130	—	185	ns	1
t_{MC}	Clocked Multiply Time	—	55	—	90	—	140	ns	1
t_S	X, Y, RND Set-Up Time	25	—	30	—	30	—	ns	1
t_H	X, Y, RND Hold Time	3	—	3	—	3	—	ns	1
t_{PWH}	Clock Pulse Width High	25	—	30	—	30	—	ns	1
t_{PWL}	Clock Pulse Width Low	25	—	30	—	30	—	ns	1
t_{PDP}	Output Clock to P	—	35	—	40	—	45	ns	1
t_{ENA}	3 State Enable Time(2)	—	35	—	40	—	45	ns	2
t_{DIS}	3 State Disable Time(2)	—	35	—	40	—	45	ns	2
t_S	Clock Enable Setput Time (IDT7213 only)	30	—	30	—	30	—	ns	1
t_H	Clock Enable Hold Time (IDT7213 only)	3	—	3	—	3	—	ns	1
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML(1) (IDT7212 only)	0	—	0	—	0	—	ns	1

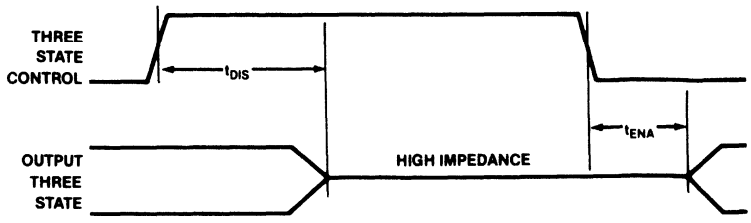
NOTES:
1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured ±500mV from steady state voltage with loading specified in Fig. 2



NOTE:
Diagram shown for HIGH data only. Output transition may be opposite sense.

DSP7212-011

Figure 3. Set-Up And Hold Time



DSP7212-012

Figure 4. Three-State Control Timing Diagram

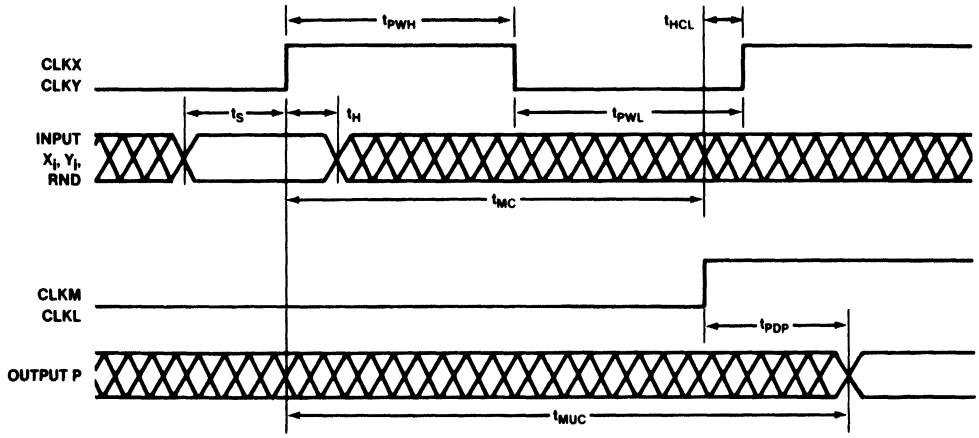


Figure 5. IDT7212 Timing Diagram

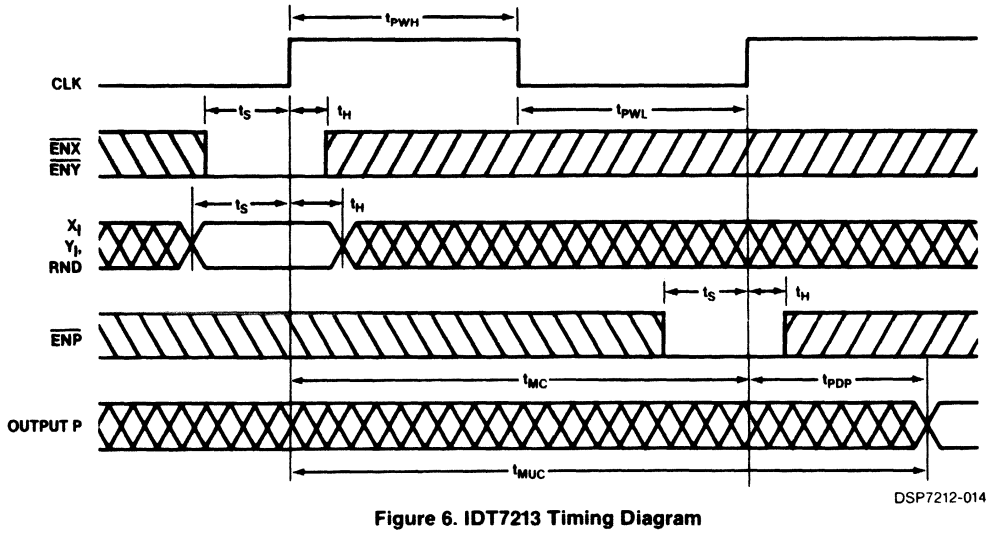


Figure 6. IDT7213 Timing Diagram

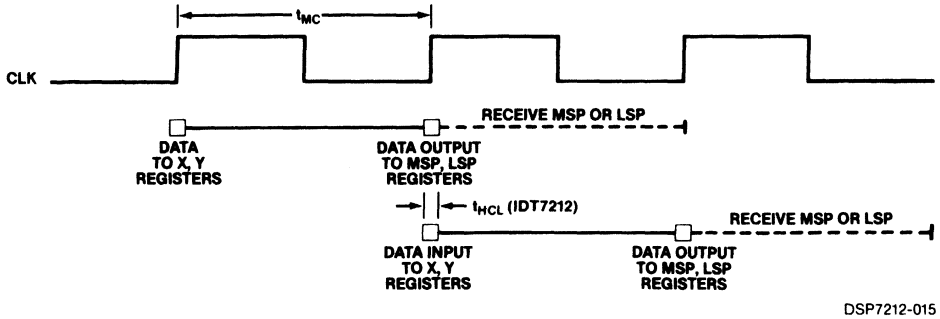


Figure 7. Simplified Timing Diagram-Typical Application

SIGNAL DESCRIPTIONS:

INPUTS:

X_{IN} (X_{11} through X_0)
Twelve Multiplicand Data Inputs

Y_{IN} (Y_{11} through Y_0)
Twelve Multiplier Data Inputs

INPUT CLOCKS (IDT7212 ONLY):

CLKX
The rising edge of this clock loads the X_{11} - X_0 data input register along with the two's complement and round registers.

CLKY
The rising edge of this clock loads the Y_{11} - Y_0 data input register along with the two's complement and round registers.

CLKM
The rising edge of this clock loads the Most Significant Product (MSP) register.

CLKL
The rising edge of this clock loads the Least Significant Product (LSP) register.

INPUT CLOCKS (IDT7213 ONLY):

CLK
The rising edge of this clock loads all registers.

$\overline{ENX}$
Register enable for the X_{11} - X_0 data input register along with the two's complement and round registers.

$\overline{ENY}$
Register enable for the Y_{11} - Y_0 data input register along with the two's complement and round registers.

$\overline{ENP}$
Register enable for the Most Significant Product (MSP) and Least Significant Product (LSP).

CONTROLS:

X_M, Y_M (TCX, TCY)[1]
Mode control inputs for each data word. A low input designates unsigned data input with a high input used for two's complement.

NOTE:
1. TRW MPY012H/K pin designation.

FA (PS)[1]
When the format adjust control is HIGH, a full 24-bit product is selected. When this control is LOW, a left-shifted 23-bit product is selected with the sign bit replicated in the Least Significant Product (LSP). This control is normally HIGH except for certain fractional two's complement applications. (See Multiplier Input/Output Formats.)

FT
When this control is HIGH, both the Most Significant Product (MSP) and Least Significant Product (LSP) registers are transparent.

$\overline{OEL}$
Three-state enable for LSP output.

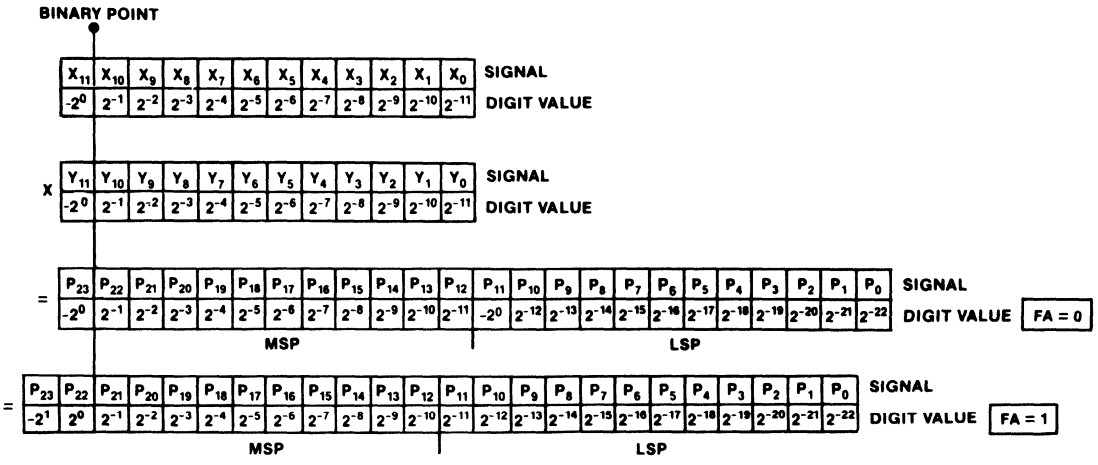
$\overline{OEP}$
Three-state enable for MSP output.

RND
Round control for the rounding of the Most Significant Product (MSP). When this control is HIGH, a one is added to the Most Significant Bit (MSB) of the Least Significant Product (LSP). Note that this bit depends on the state of the Format Adjust (FA) control. If FA is LOW when RND is HIGH, a one will be added to the 2^{-12}-bit (P_{10}). If FA is HIGH when RND is HIGH, a one will be added to the 2^{-11}-bit (P_{11}.) In either case, the LSP output will reflect this addition when RND is HIGH. Note also that rounding always occurs in the positive direction which may introduce a systematic bias. The RND input is registered and clocked in at the rising edge of the logical OR of both CLKX and CLKY.

OUTPUTS:

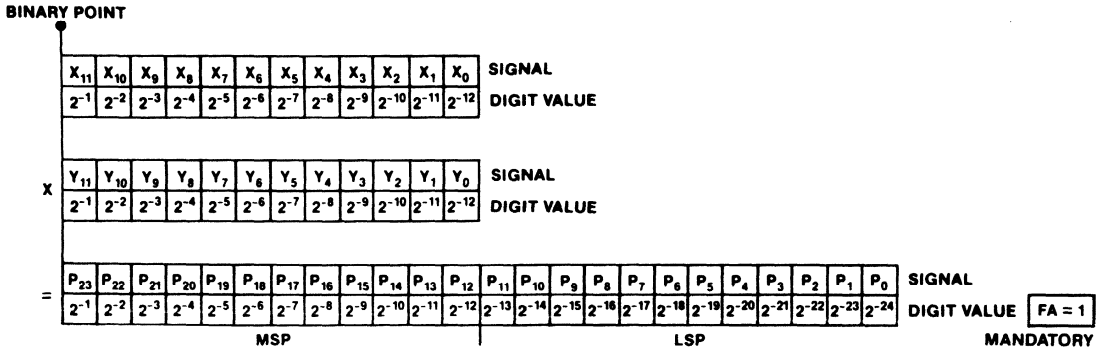
MSP (P_{23} through P_{12})
Most Significant Product Output

LSP (P_{11} through P_0)
Least Significant Product Output



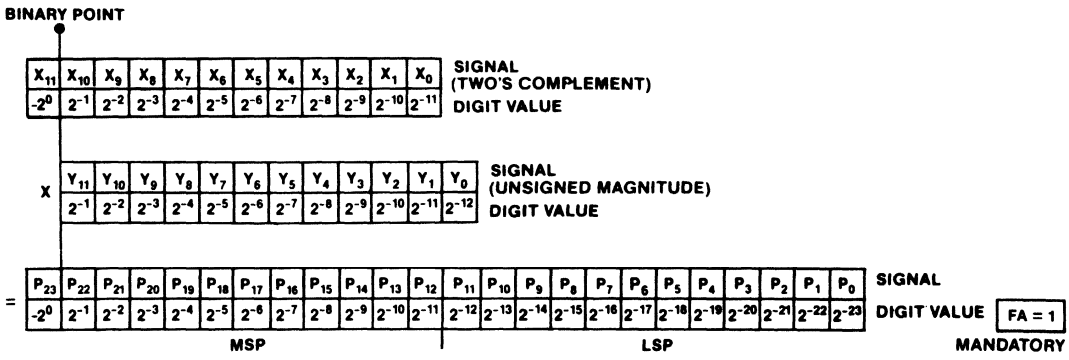
DSP7212-016

Figure 8. Fractional Two's Complement Notation



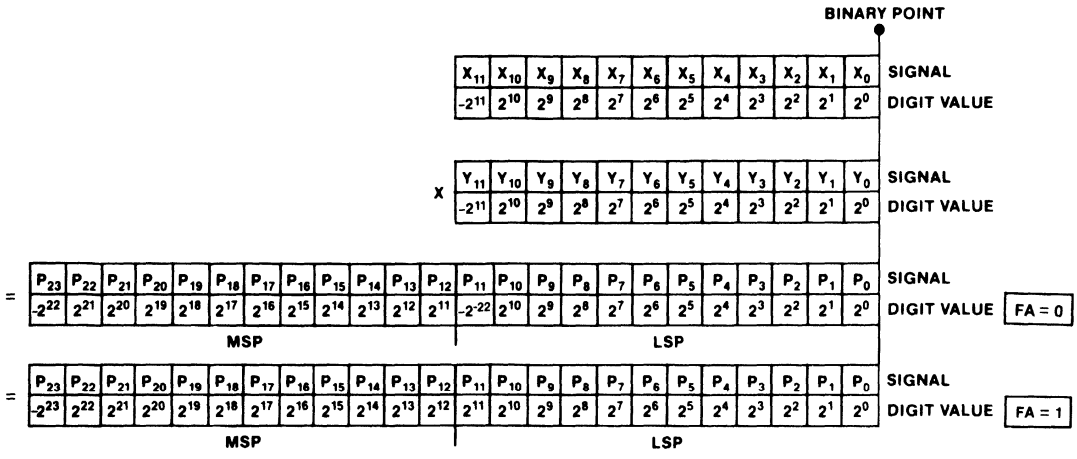
DSP7212-017

Figure 9. Fractional Unsigned Magnitude Notation



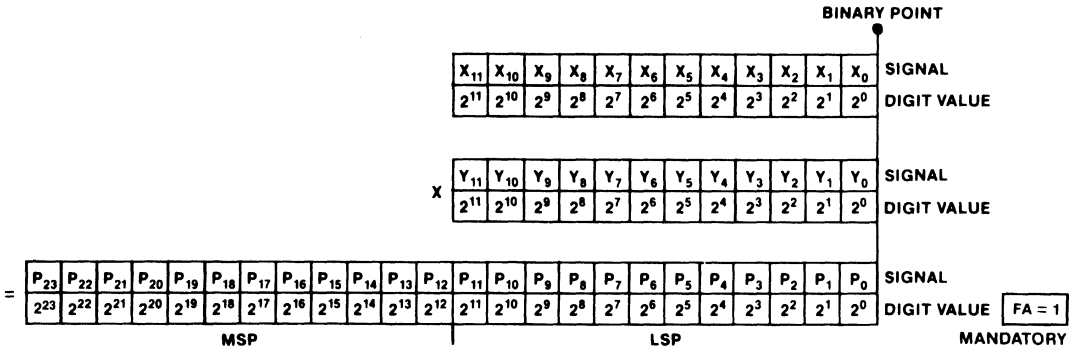
DSP7212-018

Figure 10. Fractional Mixed Mode Notation



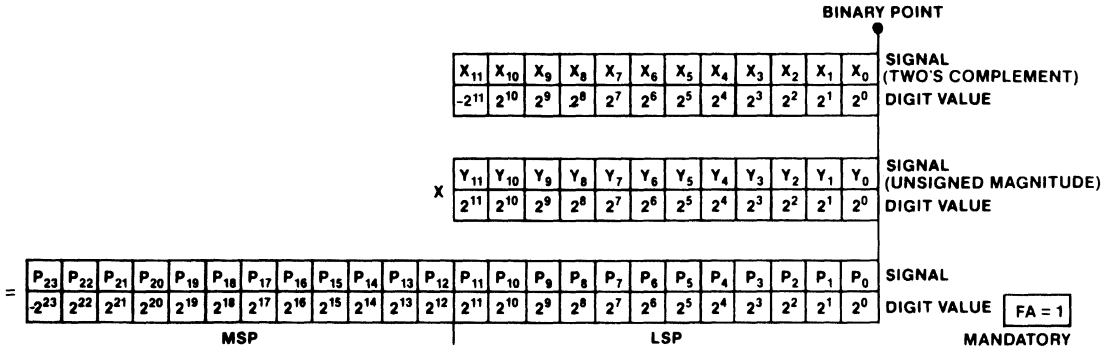
DSP7212-019

Figure 11. Integer Two's Complement Notation



DSP7212-020

Figure 12. Integer Unsigned Magnitude Notation



DSP7212-021

Figure 13. Integer Mixed Mode Notation

16 x 16 PARALLEL CMOS MULTIPLIER-ACCUMULATOR

PRELIMINARY
IDT7210
IDT7243

DSP

FEATURES:

- 16 x 16 parallel multiplier/accumulator with selectable accumulation and subtraction
- High-speed - 65ns multiply/accumulate time
- IDT7210 features selectable accumulation, subtraction, rounding and preloading with 35-bit result
- IDT7243 features selectable accumulation, subtraction and rounding with 19-bit result
- IDT7210 is pin and functionally compatible with the TRW TDC1010J
- IDT7243 is pin and functionally compatible with the TRW TDC1043
- Both devices perform subtraction and double precision addition and multiplication
- Produced using advanced sub-2 micron CEMOS™II high-performance technology
- Low power consumption (less than 250mW typical) - less than 1/15 the power of compatible bipolar and 1/7 the power of NMOS designs
- Inputs and outputs directly TTL-compatible
- Single 5V supply
- Available in DIP or LCC
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

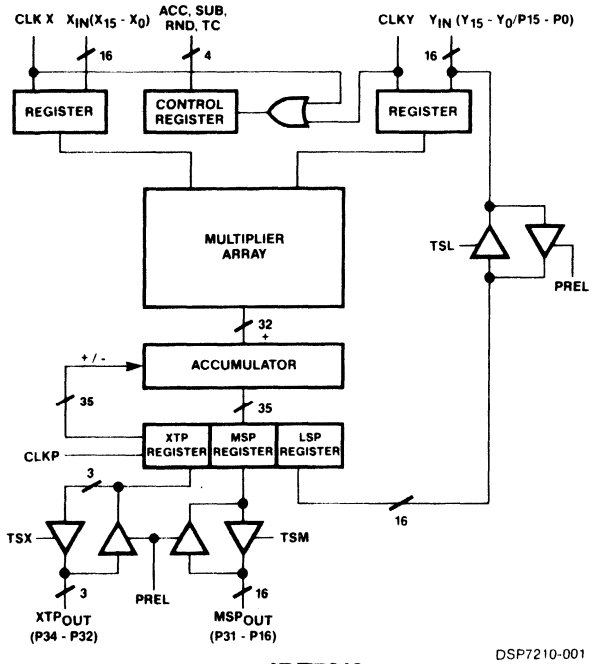
The IDT7210/7243 are high-speed, low-power 16 x 16 bit parallel multiplier/accumulators that are ideally suited for real-time digital signal processing applications. Fabricated using sub-2 micron CEMOS II silicon gate technology, these devices offer a very low power alternative to existing bipolar and NMOS counterparts with only 1/7 to 1/15 the power dissipation and exceptional speed (65ns maximum) performance.

Pin and functional replacements for TRW's TDC1010J/TDC-1043, the IDT7210/7243 operate from a single 5 volt supply and are compatible with standard TTL logic levels. The architecture of the IDT7210/7243 is fairly straightforward, featuring individual input and output registers with clocked D-type flip-flops, a pre-load capability (IDT7210 only) which enables input data to be preloaded into the output registers, individual three-state output ports for the extended product (XTP) and most significant product (MSP), and a least significant product output (LSP) which is multiplexed with the Y input. Unlike the IDT7210 the IDT7243 does not have either a preload capability or a Least Significant Product (LSP) Output.

The X_{IN} and Y_{IN} data input registers may be specified through the use of the two's complement input (TC) as either two's complement or an unsigned magnitude, yielding a full-precision 32-bit result that may be accumulated to a full 35-bit result. The

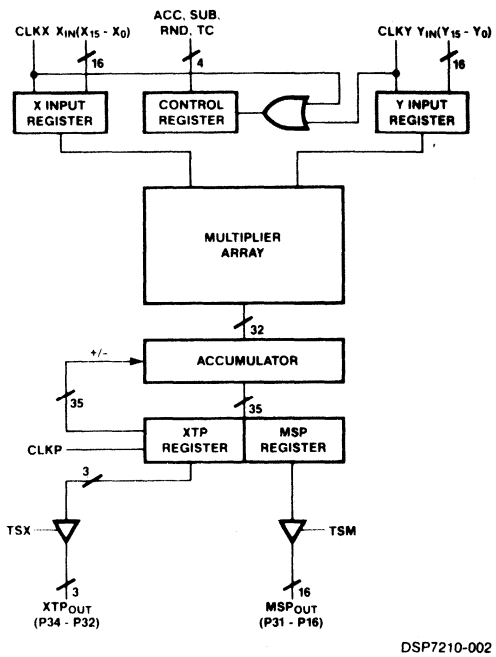
Continued on Page 2

FUNCTIONAL BLOCK DIAGRAMS



DSP7210-001

IDT7210



DSP7210-002

IDT7243

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

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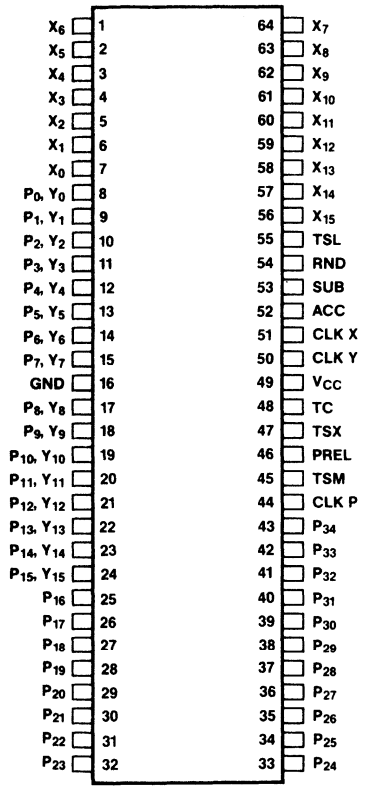
DESCRIPTION (Con't.)

three output registers—extended product (XTP), most significant product (MSP) and least significant product (LSP)—are controlled by the respective TSX, TSM and TSL input lines. The LSP output can be routed through Y_{IN} ports.

The accumulate input (ACC) enables the device to perform either a multiply or a multiply-accumulate function. In the multiply-accumulate mode, output data can be added to or subtracted from subsequent results. When the subtraction (SUB) input is active simultaneously with an active ACC, a subtraction can be performed. The double precision accumulated result is rounded down to either a single precision or single precision plus 3-bit extended result. In the multiply mode, the extended product output (XTP) is sign extended in the two's complement mode, or set to zero in the unsigned mode. The ROUND (RND) control rounds up the most significant product (MSP) and the 3-bit extended product (XTP) outputs. When pre-load input (PREL) is active, all the output buffers are forced into a high-impedance state (see PRELOAD truth table) and external data can be loaded into the output register by using the TSX, TSL and TSM signals as input controls.

PIN CONFIGURATIONS

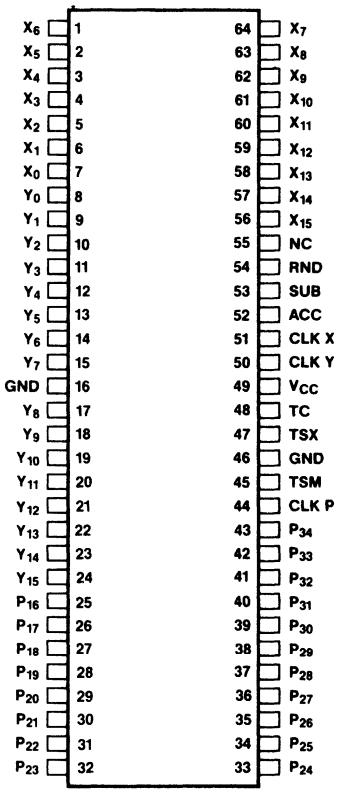
IDT7210 MULTIPLIER-ACCUMULATOR
64-PIN DIP



DSP7210-003

TOP VIEW

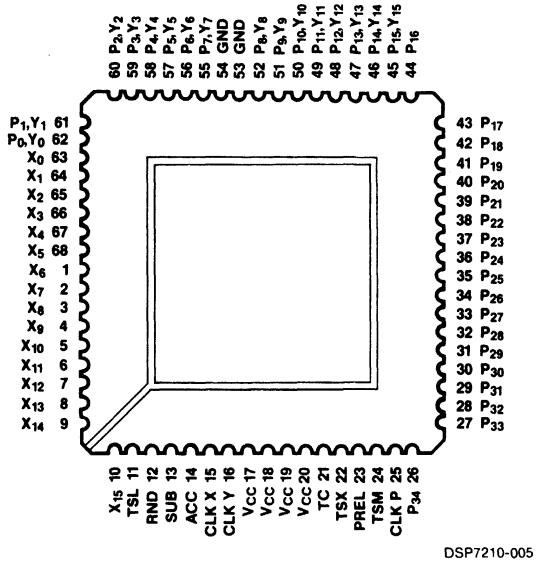
IDT7243 MULTIPLIER-ACCUMULATOR
64-PIN DIP



DSP7210-004

TOP VIEW

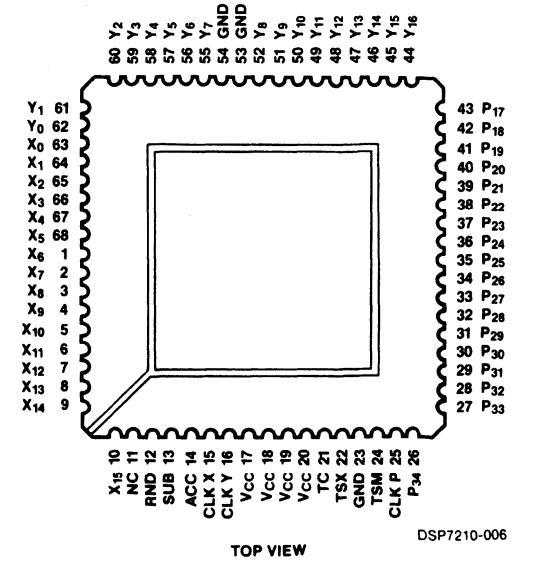
IDT7210 MULTIPLIER-ACCUMULATOR
68-PIN LCC



DSP7210-005

TOP VIEW

IDT7243 MULTIPLIER-ACCUMULATOR
68-PIN LCC



DSP7210-006

TOP VIEW

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}	Input Low Voltage	—	—	0.8	V

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliablility.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 5%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	TEST CONDITIONS	t_{MA} = 65, 75ns COMMERCIAL MIN.	TYP.(1)	MAX.	t_{MA} = 75, 85ns MILITARY MIN.	TYP.(1)	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	75	—	—	100	µA
$\|I_{LO}\|$	Output Leakage Current	High Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	—	—	75	—	—	100	µA
I_{CC}(2)	Operating Power Supply Current	Output Open	—	50	120	—	50	140	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	50	—	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - .2V or ≤ .2V	—	4	20	—	4	25	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -0.4mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0mA	—	—	0.5	—	—	0.5	V

SYMBOL	PARAMETER	TEST CONDITIONS	t_{MA} = 100, 165ns COMMERCIAL MIN.	TYP.(1)	MAX.	t_{MA} = 120, 200ns MILITARY MIN.	TYP.(1)	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	2	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	High Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	—	—	2	—	—	10	µA
I_{CC}(2)	Operating Power Supply Current	Output Open	—	40	110	—	40	130	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	10	30	—	10	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - .2V or ≤ .2V	—	0.1	1.0	—	0.1	2.0	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -0.4mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0mA	—	—	0.5	—	—	0.5	V

NOTES:
1. V_{CC} = 5V, T_A = +25°C.
2. I_{CC} is measured at maximum clock cycle and V_{IN} = TTL voltage.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

CAPACITANCE (T_A = +25°C, f = 1.0MHz)(1)

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

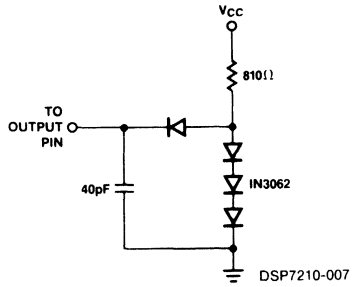


Figure 1. AC Output Test Load

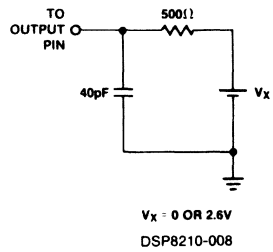


Figure 2. Output Three State Delay Load

AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ± 5%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7210-65 IDT7243-65 MIN.	MAX.	IDT7210-75 IDT7243-75 MIN.	MAX.	IDT7210-100 IDT7243-100 MIN.	MAX.	IDT7210-165 IDT7243-165 MIN.	MAX.	UNIT	TEST LOAD FIGURE
t_{MA}	Multiply - Accumulate Time	—	65	—	75	—	100	—	165	ns	1
t_D	Output Delay	—	35	—	35	—	40	—	40	ns	1
t_{ENA}	Three-State Output Enable Delay(1)	—	35	—	35	—	40	—	40	ns	2
t_{DIS}	Three-Stage Output Disable Delay(1)	—	30	—	30	—	35	—	35	ns	2
t_S	Input Register Setup Time	25	—	25	—	25	—	25	—	ns	—
t_H	Input Register Hold Time	3	—	3	—	0	—	0	—	ns	—
t_{PW}	Clock Pulse Width	25	—	25	—	25	—	25	—	ns	—

AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7210-75 IDT7243-75 MIN.	MAX.	IDT7210-85 IDT7243-85 MIN.	MAX.	IDT7210-120 IDT7243-120 MIN.	MAX.	IDT7210-200 IDT7243-200 MIN.	MAX.	UNIT	TEST LOAD FIGURE
t_{MA}	Multiply - Accumulate Time	—	75	—	85	—	120	—	200	ns	1
t_D	Output Delay	—	40	—	40	—	45	—	45	ns	1
t_{ENA}	Three-State Output Enable Delay(1)	—	40	—	40	—	45	—	45	ns	2
t_{DIS}	Three-Stage Output Disable Delay(1)	—	40	—	40	—	45	—	45	ns	2
t_S	Input Register Setup Time	30	—	30	—	30	—	30	—	ns	—
t_H	Input Register Hold Time	3	—	3	—	0	—	0	—	ns	—
t_{PW}	Clock Pulse Width	30	—	30	—	30	—	30	—	ns	—

NOTE:
1. Transition is measured ±500mV from steady state voltage with loading specified in Fig. 2.

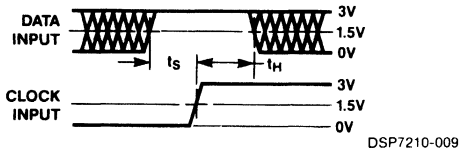


Figure 3. Set Up and Hold Time

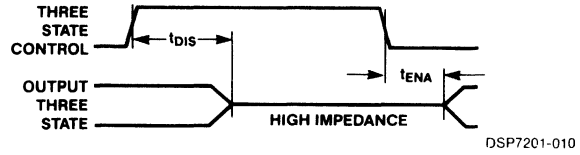


Figure 4. Three State Control Timing Diagram

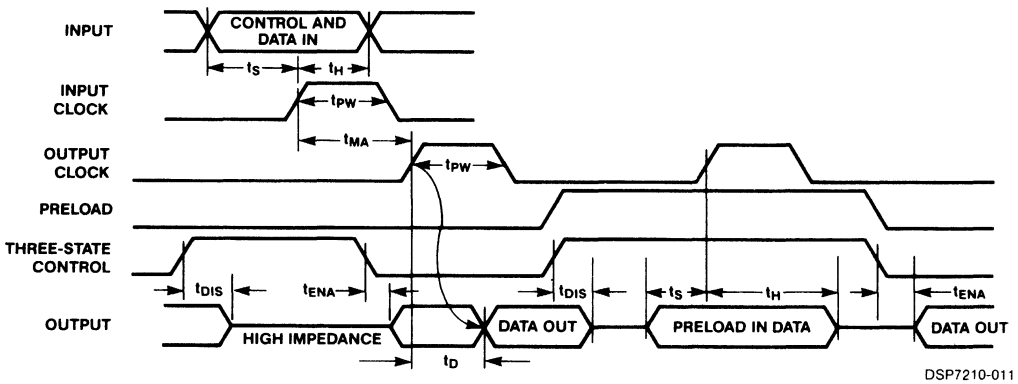


Figure 5. Timing Diagram

SIGNAL DESCRIPTIONS:

INPUTS:

X_{IN} (X_{15}-X_0)
Multiplicand Data Inputs

Y_{IN} (Y_{15}-Y_0)
Multiplier Data Inputs

INPUT CLOCKS:

CLKX, CLKY
Input data is loaded on the rising edge of these clocks.

CONTROLS:

ACC (Accumulate)
When ACC is high, the contents of the XTP, MSP and LSP registers are added to or subtracted from the multiplier output. When ACC is low, the device acts as a simple multiplier with no accumulation being performed and the next product generated will be stored directly into the output registers. The ACC signal is loaded on the rising edge of the CLKX or CLKY and must be valid for the duration of the data input.

SUB (Subtract)

When the ACC and SUB signals are both high, the contents of the output register are subtracted from the next product generated and the difference is stored back into the output registers at the rising edge of the next CLKP. When ACC is high and SUB is low, an addition instead of a subtraction is performed. Like the ACC signal, the SUB signal is loaded into the SUB register at the rising edge of either CLKX or CLKY and must be valid over the same period as the input data is valid. When the ACC is low, SUB acts as a "don't care" input.

RND (Round)

A high level at this input adds a "1" to the most significant bit of the LSP to round up the XTP and MSP data. RND, like ACC and SUB, is loaded on the rising edge of either CLKX or CLKY and must be valid for the duration of the input data.

PREL (Preload)

When the PREL input is high, the output is driven to a high impedance state. When the TSX, TSL and TSM inputs are also high, the contents of the output register can be preset to the preload data applied to the output pins at the rising of CLKP. The PREL, TSM, TSL and TSX inputs must all be valid over the same period that the preload input is valid.

Y_{IN}/LSP Output - (IDT7210 only)

Shares functions between 16-bit data input (Y_{IN}) and the least significant product output (LSP).

TSX, TSL, TSM (Three State Output Controls)

The XTP, MSP and LSP registers are controlled by direct non-registered control signals. These output drivers are at high impedance (disabled) when control signals TSX, TSM and TSL are high and are enabled when TSX, TSM and TSL are low.

OUTPUT CLOCK:

CLKP

Output data is loaded into the output register on the rising edge of this clock.

OUTPUTS:

XTP (P_{34}-P_{32})

Extended Product Output (3-bits)

MSP (P_{31}-P_{16})

Most Significant Product

LSP (P_{15}-P_0)

Least Significant Product (IDT7210 only)

NOTES ON TWO'S COMPLEMENT FORMATS:

1. In two's complement notation, the location of the binary point that signifies the separation of the fractional and integer fields is just after the sign, between the sign bit (-2^0) and the next significant bit for the multiplier inputs. This same format is carried over to the output format, except that the extended significance of the integer field is provided to extend the utility of the accumulator. In the case of the output notation, the output binary point is located between the 2^0 and 2^{-1} bit positions. The location of the binary point is arbitrary, as long as there is consistency with both the input and output formats. The number field can be considered entirely integer with the binary point just to the right of the least significant bit for the input, product and the accumulated sum.

2. When in the non-accumulating mode, the first four bits (P34 to P31) will all indicate the sign of the product. Additionally, the P30 term will also indicate the sign except for one exceptional case when multiplying -1 × -1. With the additional bits that are available in this multiplier, the -1 × -1 is a valid operation that yields a +1 product.

3. In operations that require the accumulation of single products or sum of products, there is no change in format. To allow for a valid summation beyond that available for a single multiplication product, three additional significant bits (guard bits) are provided. This is the same as if the product was accumulated off-chip in a separate 35-bit wide adder. Taking the sign at the most significant bit position will guarantee that the largest number field will be used. When the accumulated sum only occupies the right hand portion of the accumulator, the sign will be extended into the lesser significant bit positions.

PRELOAD TRUTH TABLE

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Hi Z
0	0	1	0	Q	Hi Z	Q
0	0	1	1	Q	Hi Z	Hi Z
0	1	0	0	Hi Z	Q	Q
0	1	0	1	Hi Z	Q	Hi Z
0	1	1	0	Hi Z	Hi Z	Q
0	1	1	1	Hi Z	Hi Z	Hi Z
1	0	0	0	Hi Z	Hi Z	Hi Z
1	0	0	1	Hi Z	Hi Z	PL
1	0	1	0	Hi Z	PL	Hi Z
1	0	1	1	Hi Z	PL	PL
1	1	0	0	PL	Hi Z	Hi Z
1	1	0	1	PL	Hi Z	PL
1	1	1	0	PL	PL	Hi Z
1	1	1	1	PL	PL	PL

NOTES:
HI Z = Output buffers at high impedance (output disabled).
Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.
PL = Output buffers at high impedance, or output disabled. Preload data supplied externally at output pins will be loaded into the output register at the rising edge of CLKP.

Figure 6. Fractional Two's Complement Notation

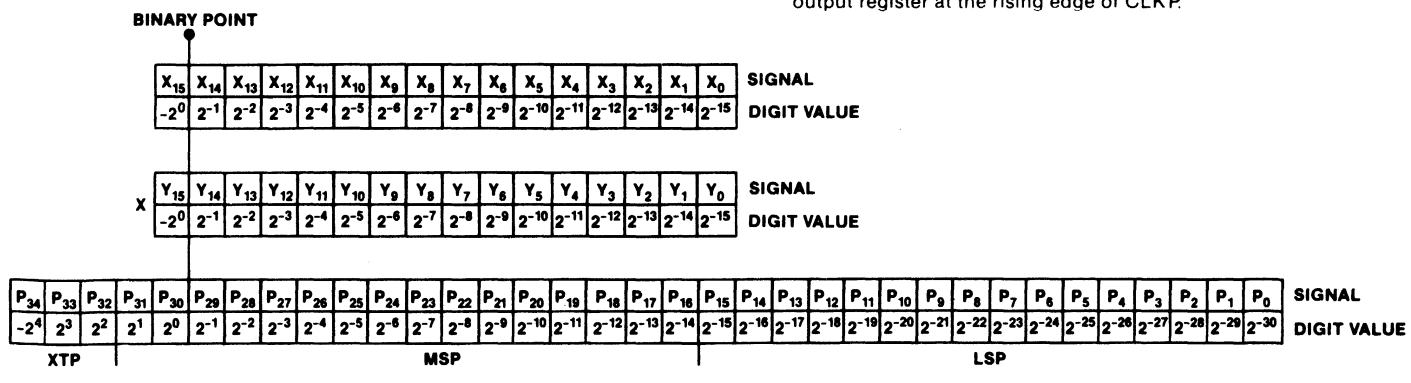


Figure 7. Fractional Unsigned Magnitude Notation

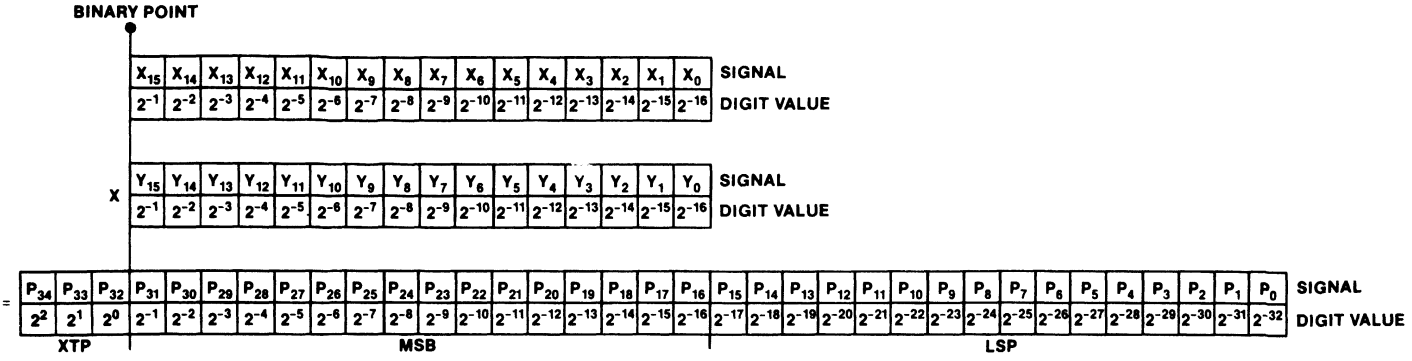


Figure 8. Integer Two's Complement Notation

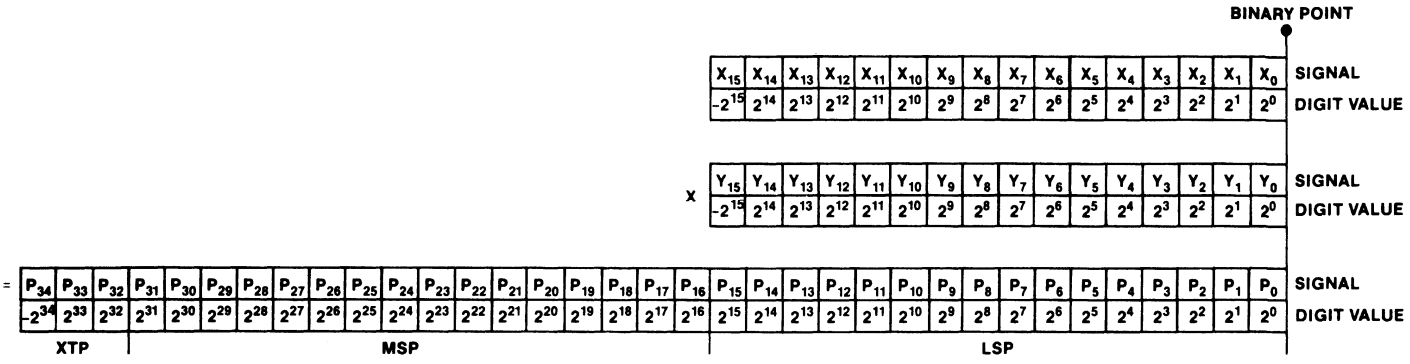
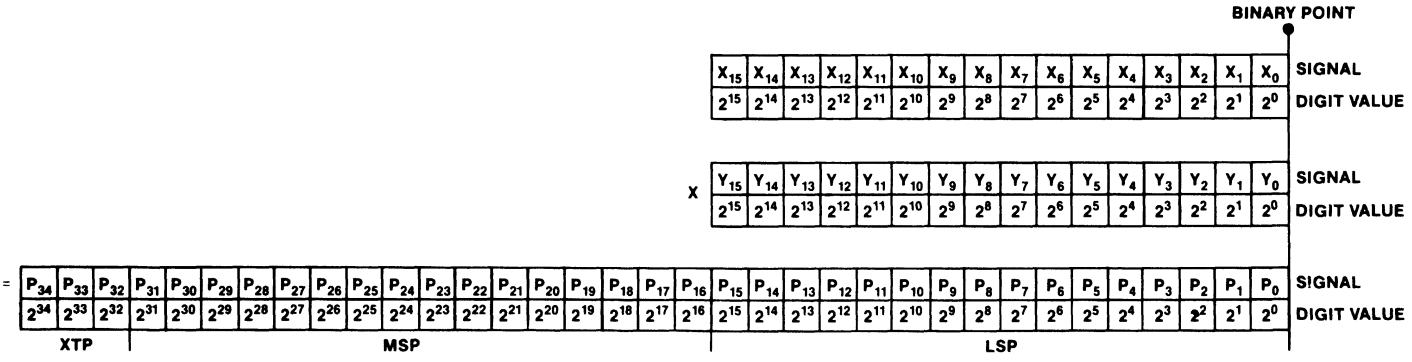


Figure 9. Integer Unsigned Magnitude Notation



Integrated Device Technology Inc

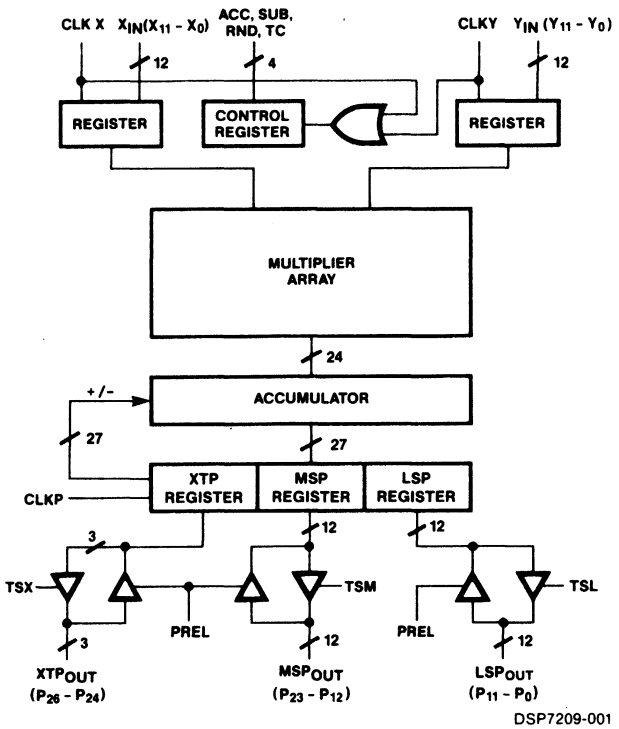
12 x 12 PARALLEL CMOS MULTIPLIER-ACCUMULATOR

PRELIMINARY
IDT7209

FEATURES:

- 12x12 parallel multiplier/accumulator with selectable accumulation and subtraction
- High-speed - 55ns maximum multiply/accumulate time
- Selectable accumulation, subtraction, rounding and preloading with 27-bit result
- Pin and functionally compatible with the TRW TDC1009J
- Performs subtraction and double precision addition and multiplication
- Produced using advanced sub-2 micron CEMOS™ II high-performance technology
- Low power consumption (less than 250mW typical) - less than 1/15 the power of compatible bipolar and 1/7 the power of NMOS designs
- Inputs and outputs directly TTL-compatible
- Single 5V supply
- Available in DIP or LCC
- Military product 100% screened to MIL-STD-883, Class B

FUNCTIONAL BLOCK DIAGRAM



DSP7209-001

IDT7209

DESCRIPTION:

The IDT7209 is a high-speed, low-power 12x12 bit parallel multiplier/accumulator that is ideally suited for real-time digital signal processing applications. Fabricated using sub-2 micron CEMOS II silicon gate technology, this device offers a very low power alternative to existing bipolar and NMOS counterparts with only 1/7 to 1/15 the power dissipation and exceptional speed (55ns maximum) performance.

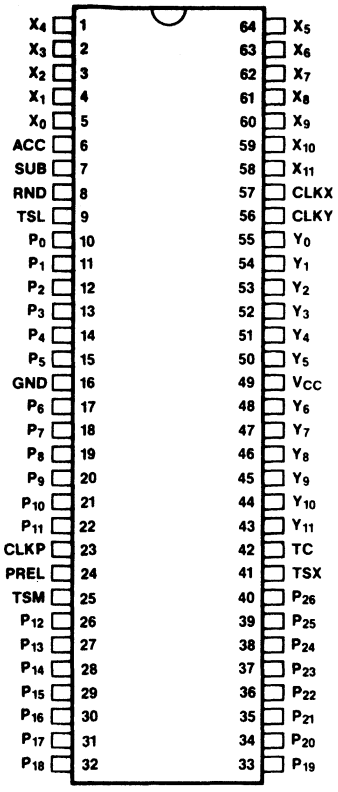
A pin and functional replacement for TRW's TDC1009J, the IDT7209 operates from a single 5 volt supply and is compatible with standard TTL logic levels. The architecture of the IDT7209 is fairly straightforward, featuring individual input and output registers with clocked D-type flip-flops, a preload capability which enables input data to be preloaded into the output registers, individual three-state output ports for the extended product (XTP) and most significant product (MSP), and a least significant product (LSP) output.

The X_{IN} and Y_{IN} data input registers may be specified through the use of the two's complement input (TC) as either two's complement or an unsigned magnitude, yielding a full-precision 24-bit result that may be accumulated to a full 27-bit result. The three output registers—extended product (XTP), most significant product (MSP) and least significant product (LSP)—are controlled by the respective TSX, TSM and TSL input lines.

The accumulate input (ACC) enables the device to perform either a multiply or a multiply-accumulate function. In the multiply-accumulate mode, output data can be added to or subtracted from subsequent results. When the subtraction (SUB) input is active simultaneously with an active ACC, a subtraction can be performed. The double precision accumulated result is rounded down to either a single precision or single precision plus 3-bit extended result. In the multiply mode, the extended product output (XTP) is sign extended in the two's complement mode or set to zero in the unsigned mode. The ROUND (RND) control rounds up the most significant product (MSP) and the 3-bit extended product (XTP) outputs. When preload input (PREL) is active, all the output buffers are forced into a high-impedance state (see PRELOAD truth table) and external data can be loaded into the output register by using the TSX, TSL and TSM signals as input controls.

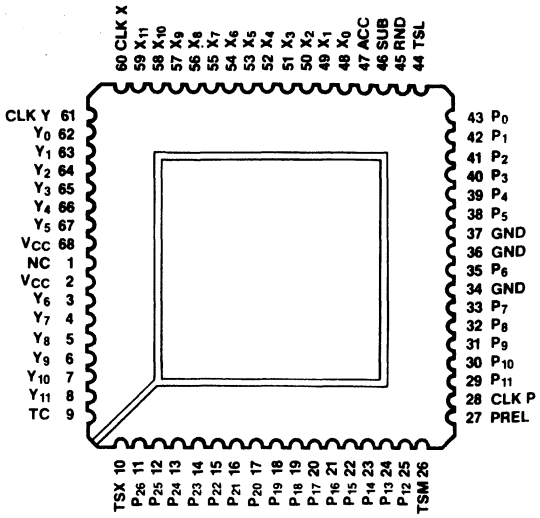
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DSP7209-002

DIP
TOP VIEW



DSP7209-003

LCC
TOP VIEW

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}	Input Low Voltage	—	—	0.8	V

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (Commercial: V_{CC} = 5V ± 5%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	TEST CONDITIONS	t_{MA} = 55, 65ns COMMERCIAL MIN.	TYP.(1)	MAX.	t_{MA} = 65, 75ns MILITARY MIN.	TYP.(1)	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0 to V_{CC}	—	—	75	—	—	100	µA
I_{LO}	Output Leakage Current	High Z, V_{CC} = max., V_{OUT} = 0 to V_{CC}	—	—	75	—	—	100	µA
I_{CC}(2)	Operating Power Supply Current	Output Open	—	50	120	—	50	140	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	50	—	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - .2V or ≤ .2V	—	4	20	—	4	25	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -0.4mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0mA	—	—	0.5	—	—	0.5	V

SYMBOL	PARAMETER	TEST CONDITIONS	t_{MA} = 100, 135ns COMMERCIAL MIN.	TYP.(1)	MAX.	t_{MA} = 120, 170ns MILITARY MIN.	TYP.(1)	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0 to V_{CC}	—	—	2	—	—	10	µA
I_{LO}	Output Leakage Current	High Z, V_{CC} = max., V_{OUT} = 0 to V_{CC}	—	—	2	—	—	10	µA
I_{CC}(2)	Operating Power Supply Current	Output Open	—	40	110	—	40	130	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	10	30	—	10	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - .2V or ≤ .2V	—	0.1	1.0	—	0.1	2.0	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -0.4mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0mA	—	—	0.5	—	—	0.5	V

NOTES:
1. V_{CC} = 5V, T_A = +25°C.
2. I_{CC} is measured at maximum clock cycle and V_{IN} = TTL voltage

DSP

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

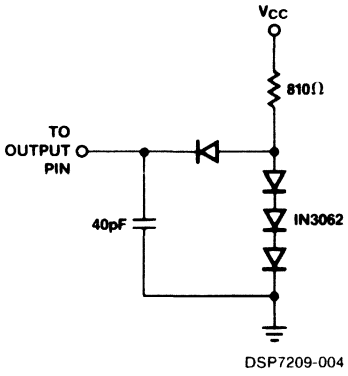


Figure 1. AC Output Test Load

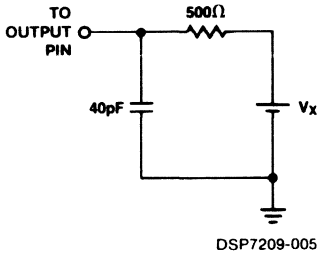


Figure 2. Output Three State Delay Load (V_X = 0V or 2.6V)

CAPACITANCE (T_A = +25°C, f = 1.0MHz)(1)

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ± 5%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7209-55		IDT7209-65		IDT7209-100		IDT7209-135		UNIT	TEST LOAD FIG.
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{MA}	Multiply - Accumulate Time	—	55	—	65	—	100	—	135	ns	1
t_D	Output Delay	—	35	—	35	—	40	—	40	ns	1
t_{ENA}	3-State Output Enable Delay(1)	—	35	—	35	—	40	—	40	ns	2
t_{DIS}	3-State Output Disable Delay(1)	—	35	—	35	—	40	—	40	ns	2
t_S	Input Register Setup Time	25	—	25	—	25	—	25	—	ns	—
t_H	Input Register Hold Time	3	—	3	—	0	—	0	—	ns	—
t_{PW}	Clock Pulse Width	25	—	25	—	25	—	25	—	ns	—

AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7209-65		IDT7209-75		IDT7209-120		IDT7209-170		UNIT	TEST LOAD FIG.
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{MA}	Multiply - Accumulate Time	—	65	—	75	—	120	—	170	ns	1
t_D	Output Delay	—	40	—	40	—	45	—	45	ns	1
t_{ENA}	3-State Output Enable Delay(1)	—	40	—	40	—	45	—	45	ns	1
t_{DIS}	3-State Output Disable Delay(1)	—	40	—	40	—	45	—	45	ns	2
t_S	Input Register Setup Time	30	—	30	—	30	—	30	—	ns	—
t_H	Input Register Hold Time	3	—	3	—	0	—	0	—	ns	—
t_{PW}	Clock Pulse Width	30	—	30	—	30	—	30	—	ns	—

NOTE:
1. Transition is measured ±500mV from steady state voltage with loading specified in Fig. 2.

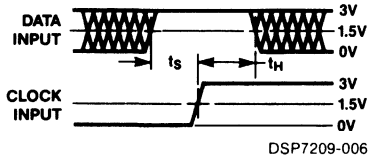


Figure 3. Set Up and Hold Time

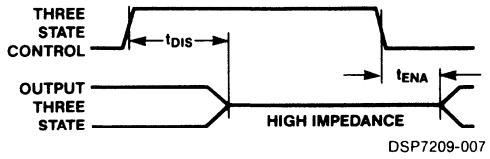


Figure 4. Three State Control Timing Diagram

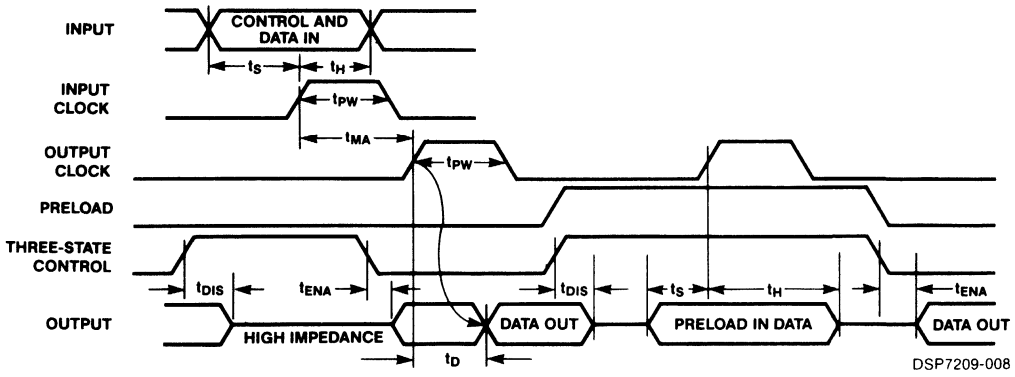


Figure 5. Timing Diagram

SIGNAL DESCRIPTIONS:

INPUTS:

X_{IN} (X_{11}-X_0)
Multiplicand Data Inputs

Y_{IN} (Y_{11}-Y_0)
Multiplier Data Inputs

INPUT CLOCKS:

CLKX, CLKY
Input data is loaded on the rising edge of these clocks.

CONTROLS:

ACC (Accumulate)
When ACC is high, the contents of the XTP, MSP and LSP registers are added to or subtracted from the multiplier output. When ACC is low, the device acts as a simple multiplier with no accumulation being performed and the next product generated will be stored directly into the output registers. The ACC signal is loaded on the rising edge of the CLKX or CLKY and must be valid for the duration of the data input.

SUB (Subtract)

When the ACC and SUB signals are both high, the contents of the output register are subtracted from the next product generated and the difference is stored back into the output registers at the rising edge of the next CLKP. When ACC is high and SUB is low, an addition instead of a subtraction is performed. Like the ACC signal, the SUB signal is loaded into the SUB register at the rising edge of either CLKX or CLKY and must be valid over the same period as the input data is valid. When the ACC is low, SUB acts as a "don't care" input.

RND (Round)

A high level at this input adds a "1" to the most significant bit of the LSP to round up the XTP and MSP data. RND, like ACC and SUB, is loaded on the rising edge of either CLKX or CLKY and must be valid for the duration of the input data.

PREL (Preload)

When the PREL input is high, the output is driven to a high impedance state. When the TSX, TSL and TSM inputs are also high, the contents of the output register can be preset to the preload data applied to the output pins at the rising of CLKP. The PREL, TSM TSL and TSX inputs must all be valid over the same period that the preload input is valid.

TSX, TSL, TSM (Three State Output Controls)

The XTP, MSP and LSP registers are controlled by direct non-registered control signals. These output drivers are at high impedance (disabled) when control signals TSX, TSM and TSL are high and are enabled when TSX, TSM and TSL are low.

OUTPUT CLOCK:

CLKP

Output data is loaded into the output register on the rising edge of this clock.

OUTPUTS:

XTP (P_{26}-P_{24})

Extended Product Output (3-bits)

MSP (P_{23}-P_{12})

Most Significant Product

LSP (P_{11}-P_0)

Least Significant Product

NOTES ON TWO'S COMPLEMENT FORMATS:

1. In two's complement notation, the location of the binary point that signifies the separation of the fractional and integer fields is just after the sign, between the sign bit (-2^0) and the next significant bit for the multiplier inputs. This same format is carried over to the output format, except that the extended significance of the integer field is provided to extend the utility of the accumulator. In the case of the output notation, the output binary point is located between the 2^0 and 2^{-1} bit positions. The location of the binary point is arbitrary, as long as there is consistency with both the input and output formats. The number field can be considered entirely integer with the binary point just to the right of the least significant bit for the input, product and the accumulated sum.

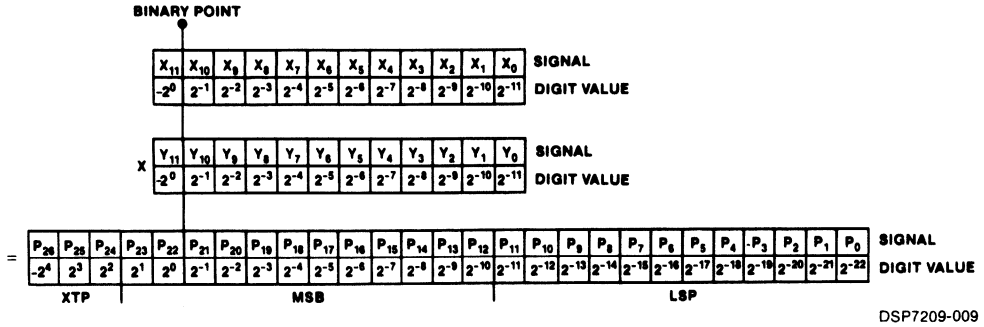
2. When in the non-accumulating mode, the first four bits (P_{26} through P_{23}) will all indicate the sign of the product. Additionally, the P_{22} term will also indicate the sign except for one exceptional case when multiplying -1×-1. With the additional bits that are available in this multiplier, the -1×-1 is valid operation that yields a +1 product.

3. In operations that require the accumulation of single products or sum of products, there is no change in format. To allow for a valid summation beyond that available for a single multiplication product, three additional significant bits (guard bits) are provided. This is the same as if the product was accumulated off-chip in a separate 27-bit wide adder. Taking the sign at the most significant bit position will guarantee that the largest number field will be used. When the accumulated sum only occupies the right hand portion of the accumulator, the sign will be extended into the lesser significant bit positions.

PRELOAD TRUTH TABLE

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Hi Z
0	0	1	0	Q	Hi Z	Q
0	0	1	1	Q	Hi Z	Hi Z
0	1	0	0	Hi Z	Q	Q
0	1	0	1	Hi Z	Q	Hi Z
0	1	1	0	Hi Z	Hi Z	Q
0	1	1	1	Hi Z	Hi Z	Hi Z
1	0	0	0	Hi Z	Hi Z	Hi Z
1	0	0	1	Hi Z	Hi Z	PL
1	0	1	0	Hi Z	PL	Hi Z
1	0	1	1	Hi Z	PL	PL
1	1	0	0	PL	Hi Z	Hi Z
1	1	0	1	PL	Hi Z	PL
1	1	1	0	PL	PL	Hi Z
1	1	1	1	PL	PL	PL

NOTES:
Hi Z = Output buffers at high impedance (output disabled).
Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.
PL = Output buffers at high impedance, or output disabled. Preload data supplied externally at output pins will be loaded into the output register at the rising edge of CLKP.



DSP7209-009

Figure 6. Fractional Two's Complement Notation

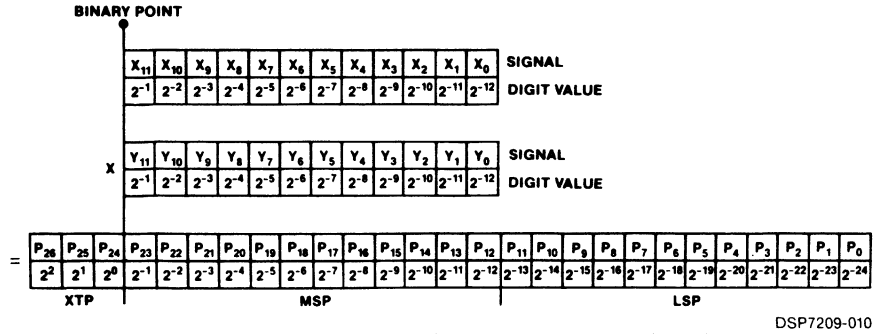


Figure 7. Fractional Unsigned Magnitude Notation

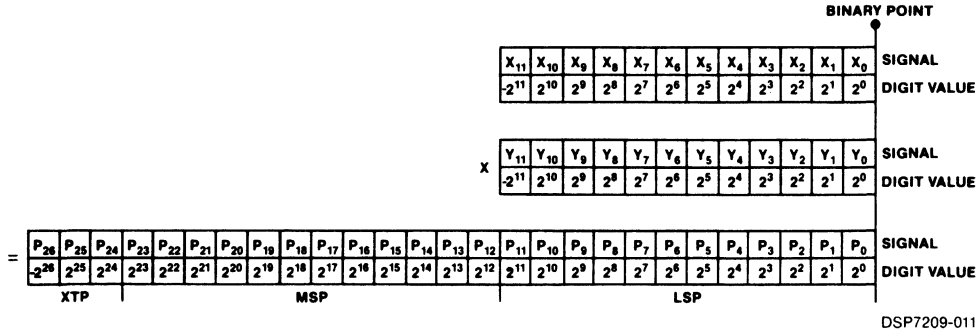


Figure 8. Integer Two's Complement Notation

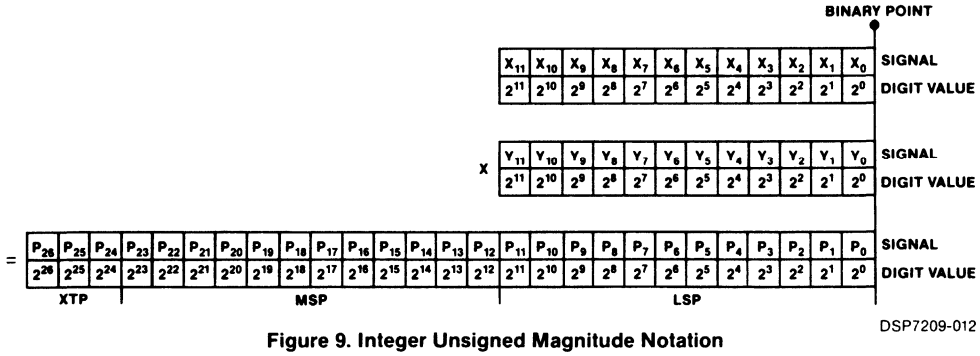


Figure 9. Integer Unsigned Magnitude Notation

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 512 x 9 BIT & 1024 x 9 BIT

IDT7201S/L
IDT7202S/L

Integrated Device Technology, Inc.

DSP

FEATURES:

- First-In, First-Out dual port memory
- 512x9 organization (IDT7201)
- 1024x9 organization (IDT7202)
- Low power consumption
  - —IDT7201/7202S Commercial:
    Active: 440mW
    Power Down: 16.5mW (Max.)
  - —IDT7201/7202S Military:
    Active: 550mW
    Power Down: 27.5mW (Max.)
  - —IDT7201/7202L Commercial:
    Active: 440mW (Max.)
    Power Down: 2.7mW (Max.)
  - —IDT7201/7202L Military:
    Active: 550mW (Max.)
    Power Down: 5mW (Max.)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- IDT7201 pin and functionally compatible with Mostek MK4501
- IDT7202 allows for deep word structure (1024) without expansion
- Half full flag capability in single device mode
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- Auto retransmit capability
- High-performance CEMOS™ II technology
- Available in DIP and LCC
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

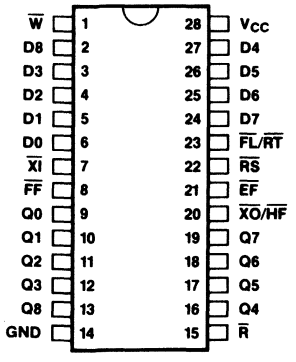
The IDT7201/7202 is a dual port memory that utilizes a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. The device uses full and empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The device has a read/write cycle time of 65ns (15MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a RETRANSMIT ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A half full flag is available in the single device mode and width expansion modes.

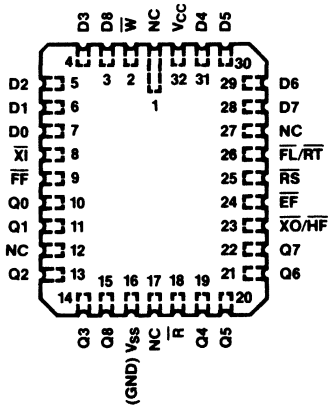
The IDT7201/7202 is fabricated using the high speed CEMOS™ II, 2 micron technology and is available in DIP and LCC screened to MIL-STD-883, Method 5004. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. The 1024x9 organization of the IDT7202 allows a 1024 deep word structure without the need for expansion.

PIN CONFIGURATIONS



DSP7201-001

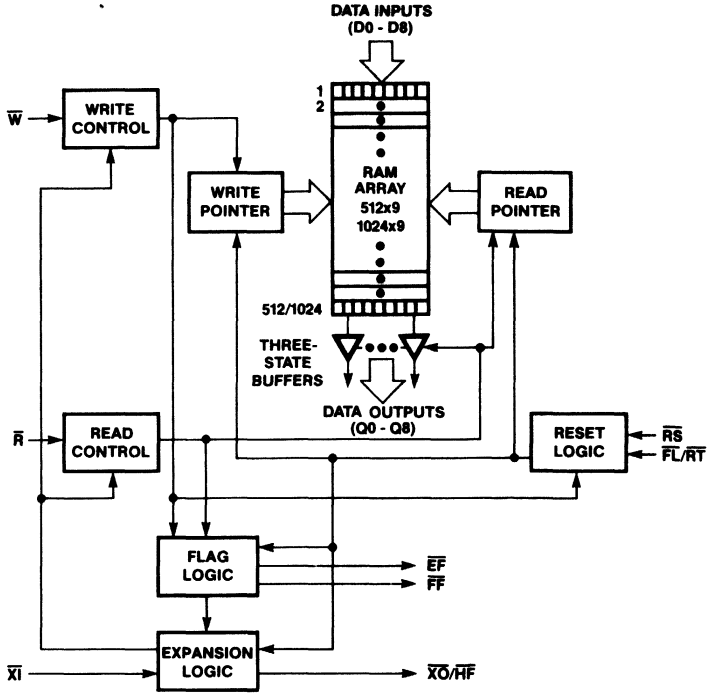
DIP
TOP VIEW



DSP7201-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



DSP7201-003

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V	—
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V	—
GND	Supply Voltage	0	0	0	V	—
V_{IH}	Input High Voltage Commercial	2.0	—	—	V	—
V_{IH}	Input High Voltage Military	2.2	—	—	V	—
V_{IL}	Input Low Voltage Commercial & Military	—	—	0.8	V	1

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7201S/L IDT7202S/L COMMERCIAL			IDT7201S/L IDT7202S/L MILITARY			UNIT	NOTES
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
I_{IL}	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	μA	1
I_{OL}	Output Leakage Current	-10	—	10	-10	—	10	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1mA	2.4	—	—	2.4	—	—	V	—
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA	—	—	0.4	—	—	0.4	V	—
I_{CC1}	Average V_{CC} Power Supply Current	—	50	80	—	70	100	mA	3
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL}/\overline{RT}$ = V_{IH})	—	5	8	—	8	15	mA	3
$I_{CC3}(L)$	Power Down Current (All Input = V_{CC} -0.2V)	—	—	500	—	—	900	μA	3
$I_{CC3}(S)$	Power Down Current (All Input = V_{CC} -0.2V)	—	—	5	—	—	9	mA	3

NOTES:
1. Measurements with $0.4 \leq V_{IN} \leq V_{OUT}$.
2. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT}$ V_{CC}.
3. I_{CC} measurements are made with outputs open.

AC ELECTRICAL CHARACTERISTICS[1] (Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

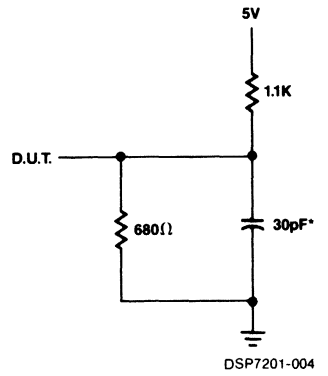
SYMBOL	PARAMETERS	7201/2-50 MIN.	7201/2-50 MAX.	7201/2-65 MIN.	7201/2-65 MAX.	7201/2-80 MIN.	7201/2-80 MAX.	7201/2-120 MIN.	7201/2-120 MAX.	UNITS	NOTES
t_{RC}	Read Cycle Time	65	—	80	—	100	—	140	—	ns	—
t_A	Access Time	—	50	—	65	—	80	—	120	ns	—
t_{RR}	Read Recovery Time	15	—	15	—	20	—	20	—	ns	—
t_{RPW}	Read Pulse Width	50	—	65	—	80	—	120	—	ns	2
t_{RLZ}	Read Pulse Low to Data Bus at Low Z	10	—	10	—	10	—	10	—	ns	3
t_{WLZ}	Write Pulse High to Data Bus at Low Z	15	—	15	—	20	—	20	—	ns	3
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns	—
t_{RHZ}	Read Pulse High to Data Bus at High Z	—	30	—	30	—	30	—	35	ns	3
t_{WC}	Write Cycle Time	65	—	80	—	100	—	140	—	ns	—
t_{WPW}	Write Pulse Width	50	—	65	—	80	—	120	—	ns	2
t_{WR}	Write Recovery Time	15	—	15	—	20	—	20	—	ns	—
t_{DS}	Data Setup Time	30	—	30	—	40	—	40	—	ns	—
t_{DH}	Data Hold Time	5	—	10	—	10	—	10	—	ns	—
t_{RSC}	Reset Cycle Time	65	—	80	—	100	—	140	—	ns	—
t_{RS}	Reset Pulse Width	50	—	65	—	80	—	120	—	ns	2
t_{RSR}	Reset Recovery Time	15	—	15	—	20	—	20	—	ns	—
t_{RTC}	Retransmit Cycle Time	65	—	80	—	100	—	140	—	ns	—
t_{RT}	Retransmit Pulse Width	50	—	65	—	80	—	120	—	ns	2
t_{RTR}	Retransmit Recovery Time	15	—	15	—	20	—	20	—	ns	—
t_{EFL}	Reset to Empty Flag Low	—	65	—	80	—	100	—	140	ns	—
t_{REF}	Read Low to Empty Flag Low	—	45	—	60	—	70	—	110	ns	—
t_{RFF}	Read High to Full Flag High	—	45	—	60	—	70	—	110	ns	—
t_{WEF}	Write High to Empty Flag High	—	45	—	60	—	70	—	110	ns	—
t_{WFF}	Write Low to Full Flag Low	—	45	—	60	—	70	—	110	ns	—
t_{WHF}	Write Low to Half Full Flag Low	—	65	—	80	—	100	—	140	ns	—
t_{RHF}	Read High to Half Full Flag High	—	65	—	80	—	100	—	140	ns	—

NOTES:

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1



*Includes jig and scope capacitances.

Figure 1. Output Load.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)[1]

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT	NOTES
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF	3
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF	2,3

NOTES:

1. This parameter is sampled and not 100% tested.
2. With output deselected.
3. Characterized values, not currently tested.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D0 - D8)

Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the RESET ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) inputs must be in the high state during reset. HALF FULL FLAG ($\overline{HF}$) will be reset to high after master RESET ($\overline{RS}$).

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the FULL FLAG ($\overline{FF}$) is not set. Data setup and hold times must be adhered to with respect to the rising edge of the WRITE ENABLE ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

After half of the memory is filled, and at the falling edge of the next write operation, the HALF FULL FLAG ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The HALF FULL FLAG ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the FULL FLAG ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the READ ENABLE ($\overline{R}$) provided the EMPTY FLAG ($\overline{EF}$) is not set. The data is accessed on a First-In, First-Out basis independent of any ongoing write operations. After READ ENABLE ($\overline{R}$) goes high, the Data Outputs (Q0 through Q8) will return to a high impedance condition until the next READ operation. When all the data has been read from the FIFO, the EMPTY FLAG ($\overline{EF}$) will go low, inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the EMPTY FLAG ($\overline{EF}$) will go high after t_{WEF}, and a valid READ can then begin.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual purpose output. In the Multiple Device Mode, this pin is grounded to indicate that it is the first device loaded. (See Operating Modes.) In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the EXPANSION IN ($\overline{XI}$).

The IDT7201/2 can be made to retransmit data when the RETRANSMIT ENABLE CONTROL ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 512/1024 writes are performed between resets. The retransmit feature is not compatible with Depth Expansion Mode and will affect HALF FULL FLAG ($\overline{HF}$) depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)

This input is a dual purpose pin. EXPANSION IN ($\overline{XI}$) is grounded to indicate an operation in the single device mode. EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

The FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location from the read pointer, indicating that the device is full. If the read pointer is not moved after RESET ($\overline{RS}$), the FULL FLAG ($\overline{FF}$) will go low after 512 writes for the IDT7201 and 1024 writes for the IDT7202.

EXPANSION OUT/HALF FULL FLAG ($\overline{XO}/\overline{HF}$)

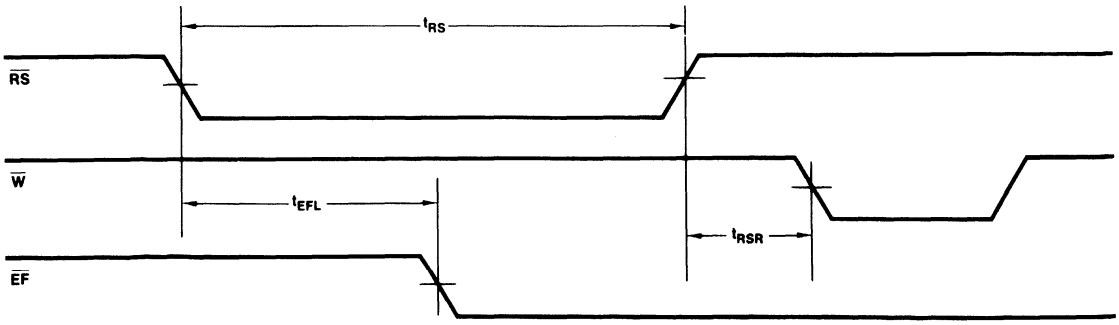
This is a dual purpose output. In the single device mode, when EXPANSION IN ($\overline{XI}$) is grounded, this output acts as an indication of a half full memory.

After half of the memory is filled, and at the falling edge of the next write operation, the HALF FULL FLAG ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The HALF FULL FLAG ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Multiple Device Mode, EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS (Q0 - Q8)

Data outputs for 9-bit wide data. This output is in a high impedance condition whenever READ ($\overline{R}$) is in a high state.



NOTES:

1. $t_{RSC} = t_{RS} + t_{RSR}$.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} during RESET.

Figure 2. Reset

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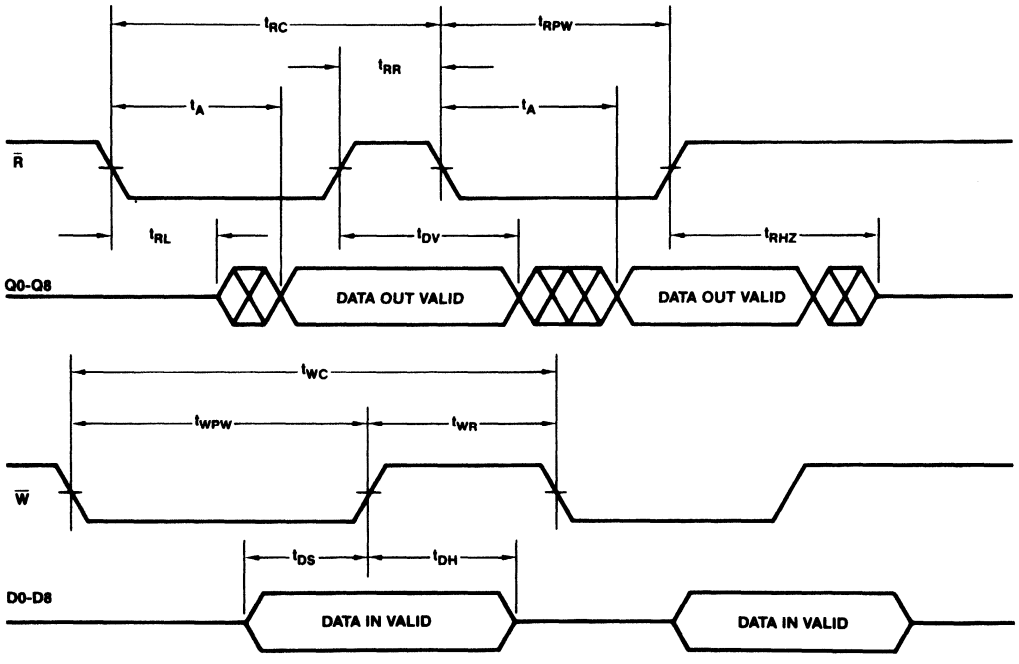


Figure 3. Asynchronous Write and Read Operation

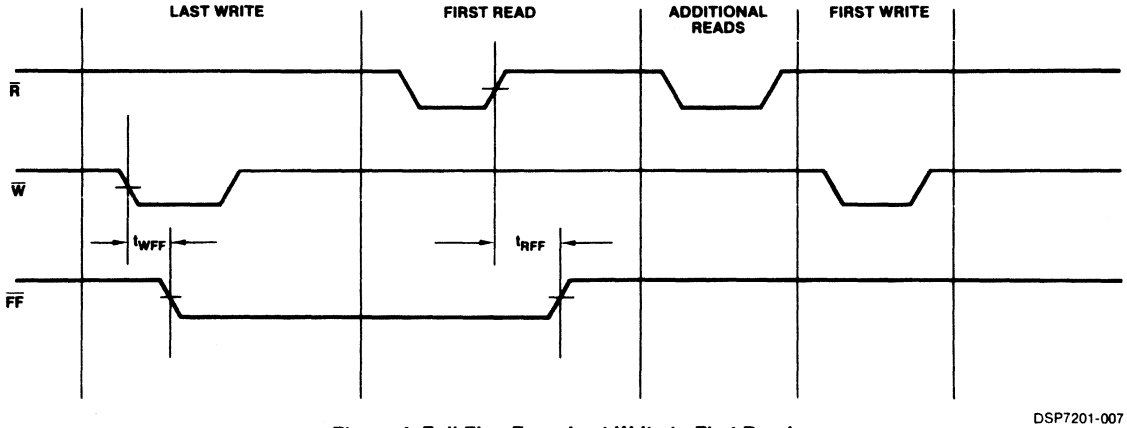


Figure 4. Full Flag From Last Write to First Read

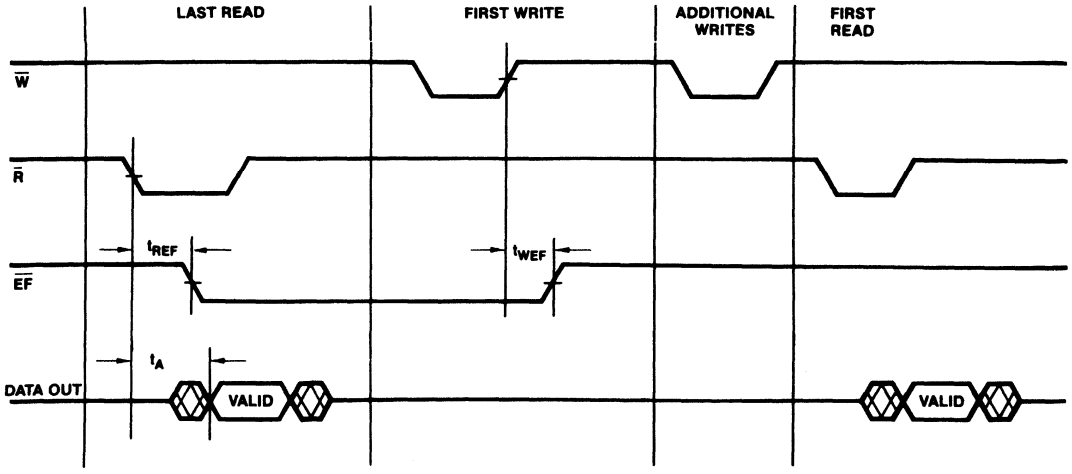
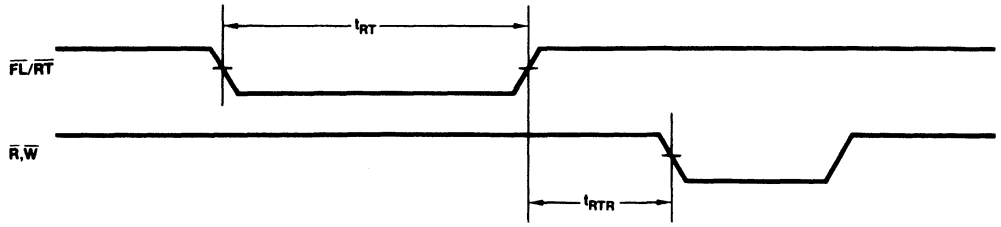


Figure 5. Empty Flag From Last Read to First Write

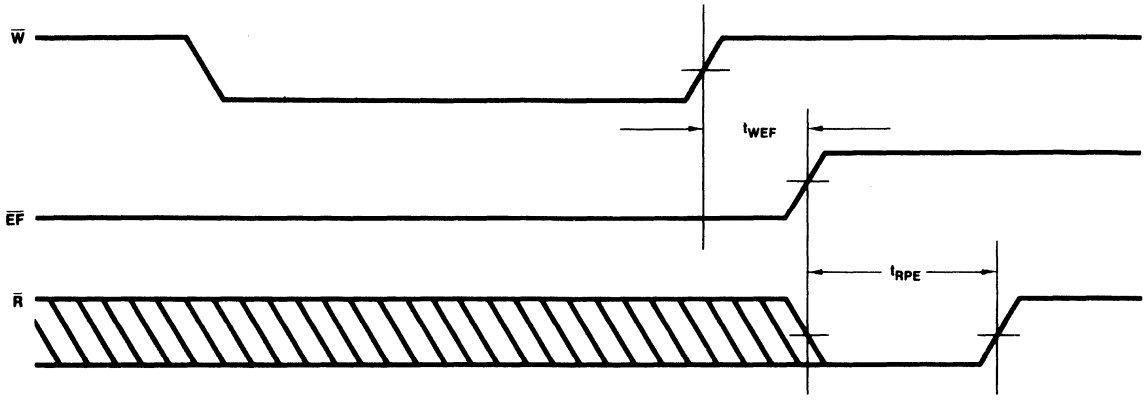


NOTES:

1. $t_{RTC} = t_{RT} + t_{RTR}$.
2. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

Figure 6. Retransmit

t_{RPE}: EFFECTIVE READ PULSE WIDTH AFTER EMPTY FLAG HIGH

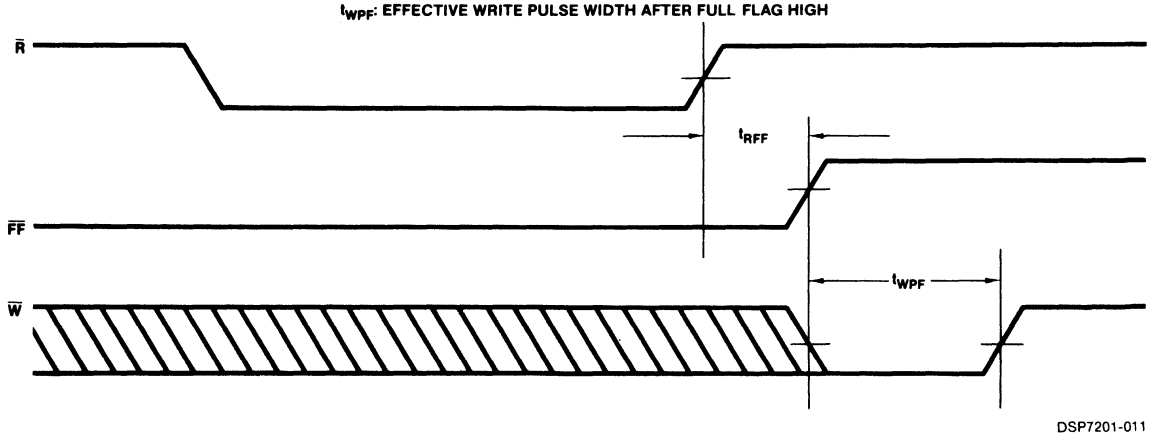


NOTE:

1. ($t_{RPE} = t_{RPW}$).

Figure 7. Empty Flag Timing

t_{WPF}: EFFECTIVE WRITE PULSE WIDTH AFTER FULL FLAG HIGH



NOTE:

1. ($t_{WPF} = t_{WPW}$).

Figure 8. Full Flag Timing

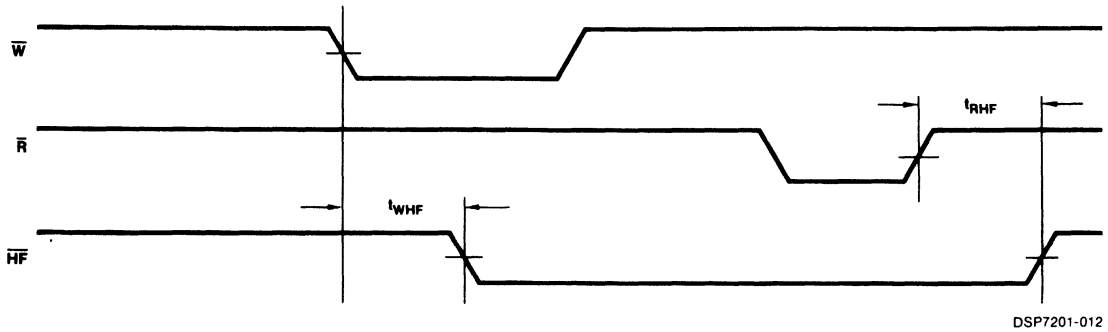


Figure 9. Half-Full Flag Timing

OPERATING MODES: SINGLE DEVICE MODE

A single IDT7201/2 may be used when the application requirements are for 512/1024 words or less. The IDT7201/2 is in a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is grounded. (See Figure 10.) In this mode the HALF FULL FLAG ($\overline{HF}$), which is an active low output, is shared with EXPANSION OUT ($\overline{XO}$).

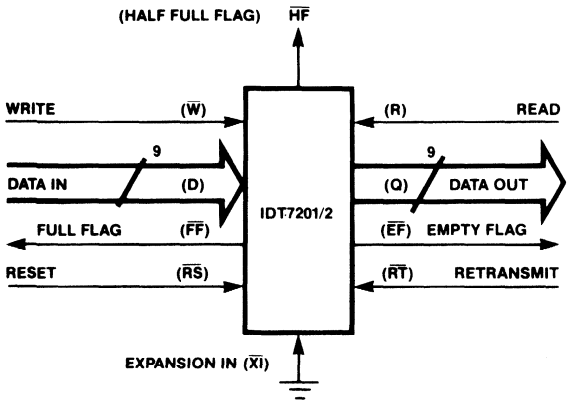


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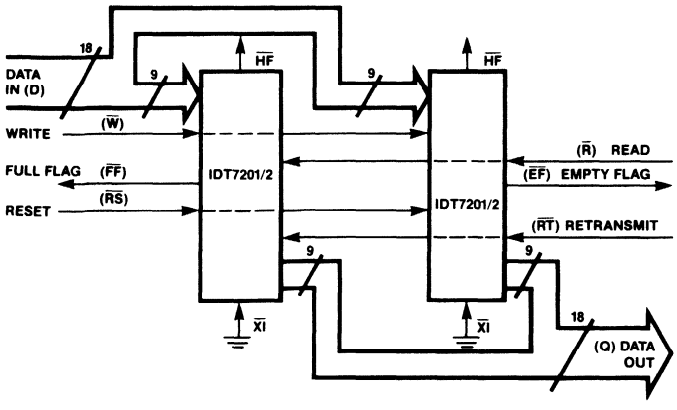
Figure 10. Block Diagram of Single 512x9/1024x9 FIFO

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 11 demonstrates an 18-bit word width by using two IDT7201/2s. Any word width can be attained by adding additional IDT7201/2s.



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NOTES:
Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, and the $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 11. Block Diagram of 512x18/1024x18 FIFO Memory Used in Width Expansion Mode

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7201/2 can easily be adapted to applications when the requirements are for greater than 512/1024 words. Figure 12 demonstrates Depth Expansion using three IDT7201/2s. Any depth can be attained by adding additional IDT7201/2s. The IDT7201/2 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the FIRST LOAD ($\overline{FL}$) control input.
2. All other device must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. See Figure 12.
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s. (I.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 12.
5. The RETRANSMIT ($\overline{RT}$) function and HALF FULL FLAG ($\overline{HF}$) are not available in the Depth Expansion Mode.

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays. (See Figure 13.)

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by pairing IDT7201/2s as is shown in Figure 14. Care must be taken to assure that the appropriate flag is monitored by each system. (I.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used.) Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW THRU MODES

Two types of flow through modes are permitted with the IDT7201/7202: A read flow through and write flow through mode. For the read flow through mode (Figure 15), the FIFO permits a reading of a single word of data immediately after writing one word of data into the completely empty FIFO.

In the write flow through mode (Figure 16), the FIFO permits a writing of a single word of data immediately after reading one word of data from a completely full FIFO.

DSP

TRUTH TABLES

TABLE I — RESET AND RETRANSMIT — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if flag is high.

TABLE II — RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12.
   $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half Full Flag Output.

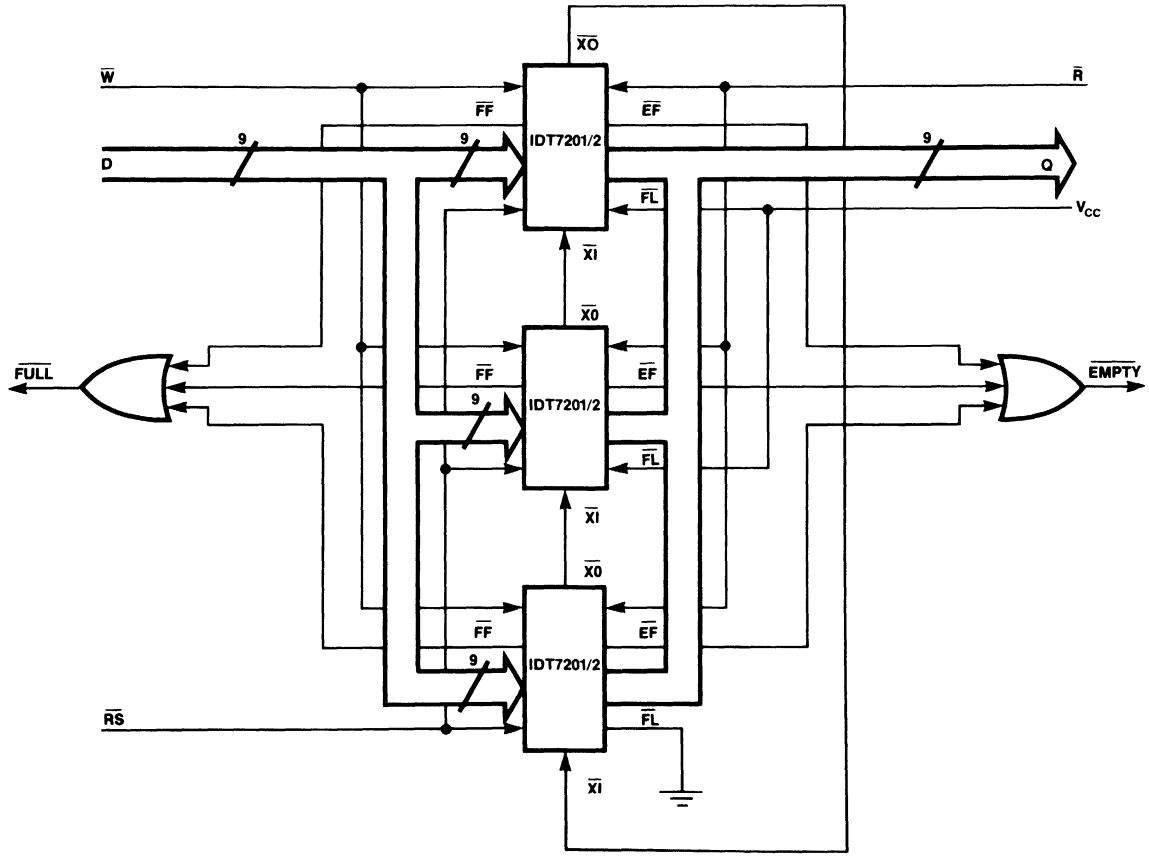

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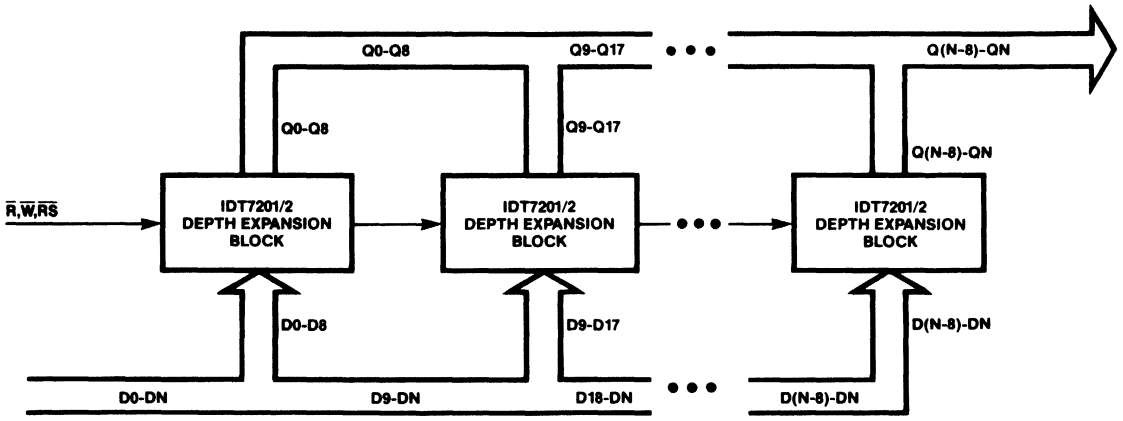
Figure 12. Block Diagram of 1536x9/3072x9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 12.
2. For Flag detection see WIDTH EXPANSION Section and Figure 11.

Figure 13. Compound FIFO Expansion

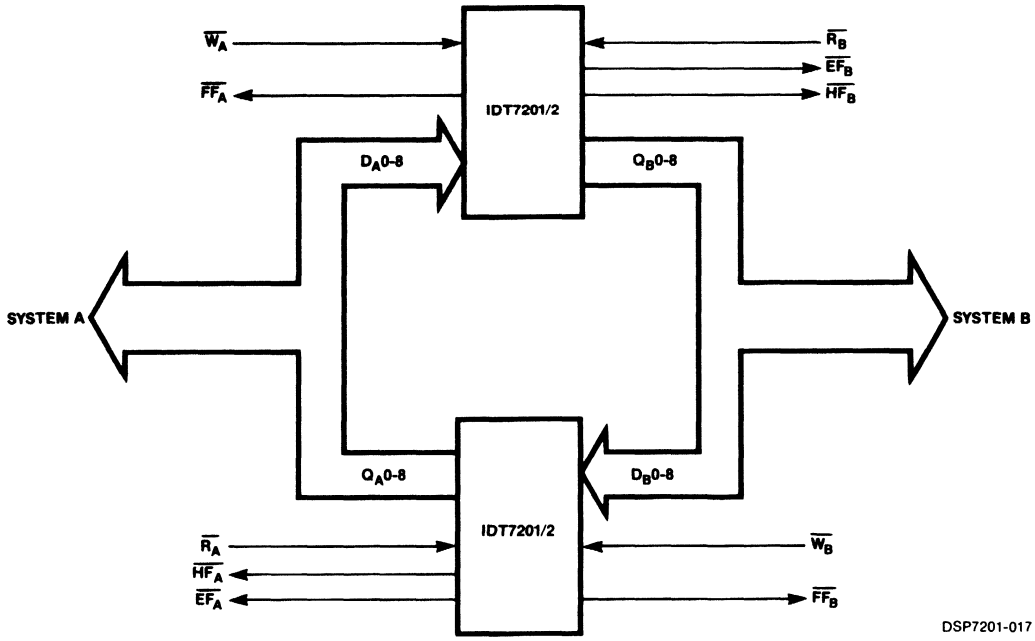


Figure 14. Bidirectional FIFO Mode

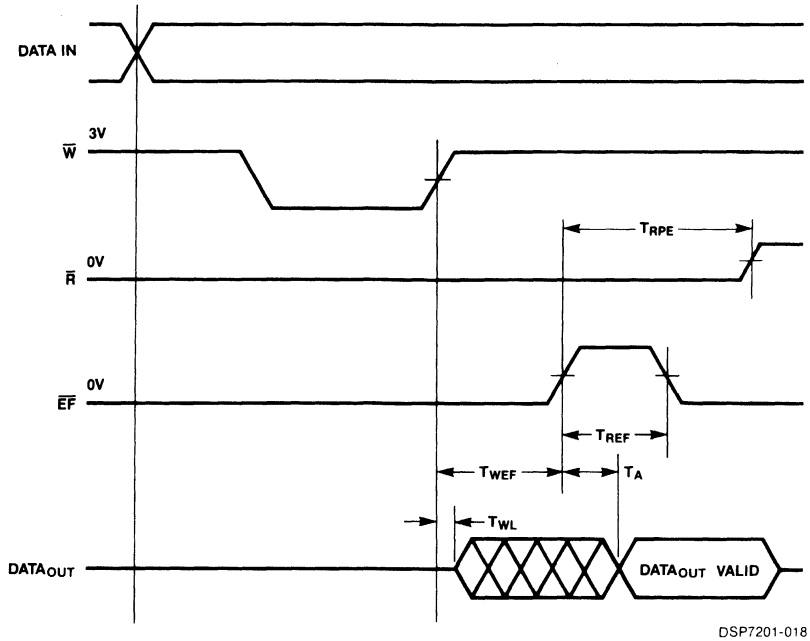


Figure 15. Read Data Flow-Through Mode

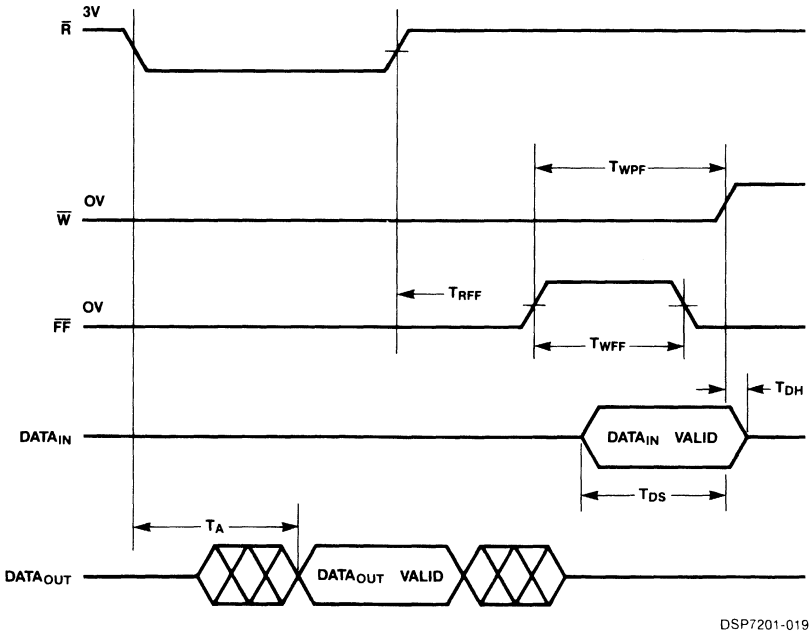


Figure 16. Write Data Flow-Through Mode

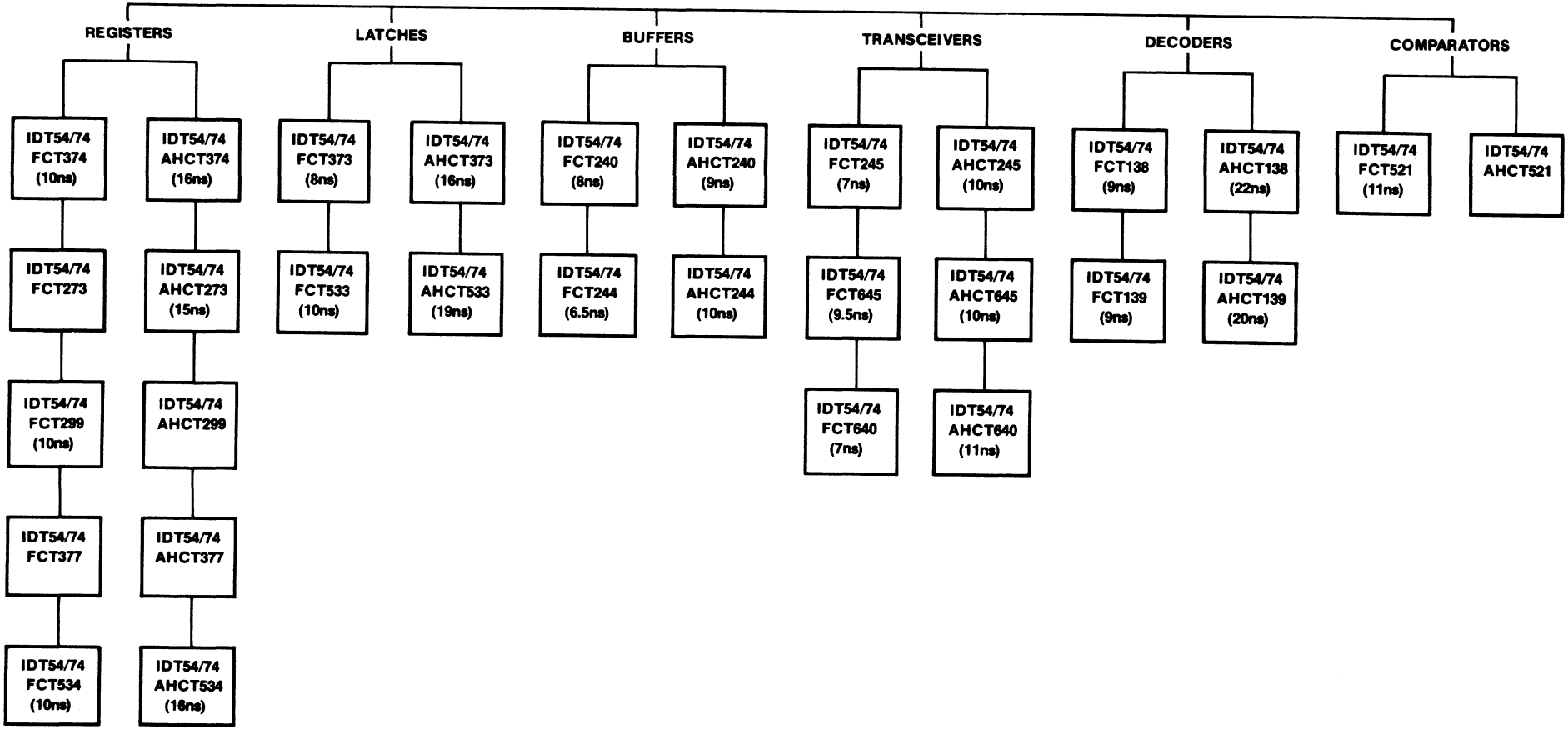
HIGH-SPEED CMOS MEMORY INTERFACE LOGIC PRODUCTS

CONTENTS **PAGE**

Integrated Device Technology, Inc.

LEADING THE CMOS FUTURE

CMOS MEMORY INTERFACE LOGIC



FCT product equivalent to FAST™ speed and output drive at CMOS power levels.
AHCT product equivalent to ALS speed and output drive at CMOS power levels.

Integrated Device Technology Inc

FAST™ CMOS 1-OF-8 DECODER

IDT54/74FCT138

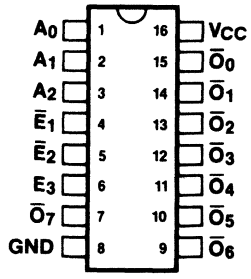
FEATURES:

- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- 7ns typical address to output delay
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- 1-of-8 decoder with enables
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

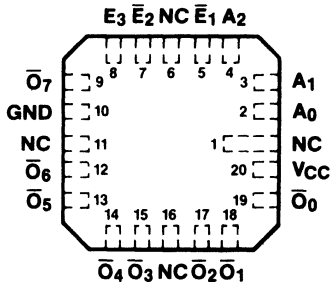
The IDT54/74FCT138 are 1-of-8 decoders built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The IDT54/74FCT138 accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The IDT54/74FCT138 features three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four IDT54/74FCT138 devices and one inverter.

PIN CONFIGURATIONS



SSDFCT138-001

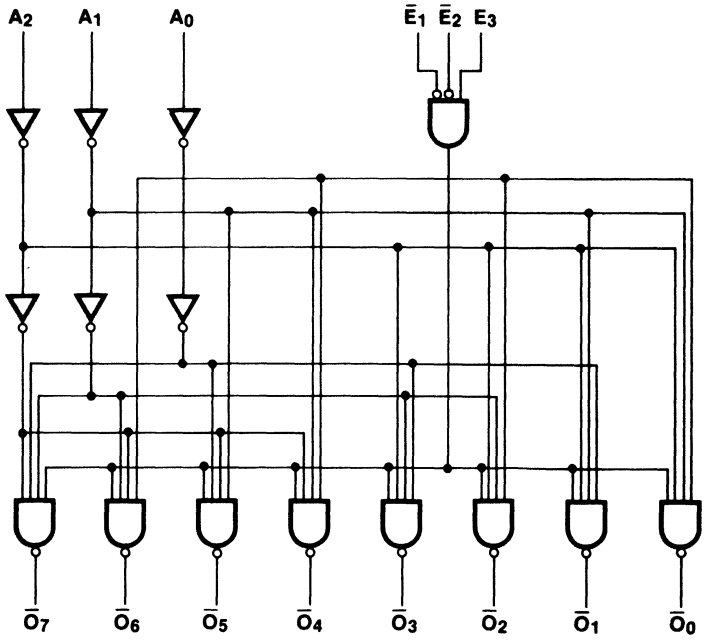
DIP
TOP VIEW



SSDFCT138-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDFCT138-003

MEMORY INTERFACE

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CEMOS is a trademark of Integrated Device Technology, Inc.

Printed in U.S.A.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	μA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32μA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300μA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL	—	0.3	0.5	
			I_{OL} = 48mA COM	—	0.3	0.5	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN} \le V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 10 MHz Outputs Open One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	1.5	5.0	mA
			V_{IN} = 3.4V[4]	—	2.0	6.3	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V).
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V).

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
A_0-A_2	Address Inputs
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
$\overline{O}_0$-$\overline{O}_7$	Outputs (Active LOW)

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A_N to $\overline{O}_N$	C_L = 50 pf R_L = 500 Ω	7.0	3.5	9.0	3.5	12.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_N$		6.0	3.0	9.0	3.0	12.5	ns
t_{PLH} t_{PHL}	Propagation Delay E_3 to $\overline{O}_N$		6.0	3.5	9.0	3.5	12.5	ns

FAST™ CMOS DUAL 1-OF-4 DECODER

IDT54/74FCT139

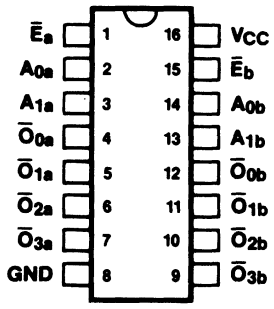
FEATURES:

- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- 6ns typical address to output delay
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Dual 1-of-4 decoder with enable
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

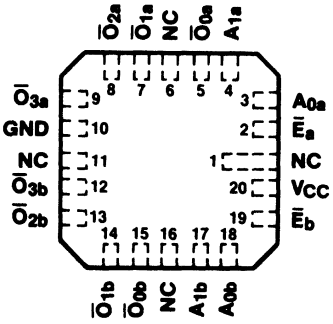
The IDT54/74FCT139 are dual 1-of-4 decoders built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The device has two independent decoders, each of which accepts two binary weighed inputs (A_0-A_1) and provides four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH, all outputs are forced HIGH.

PIN CONFIGURATIONS



SSDFCT139-001

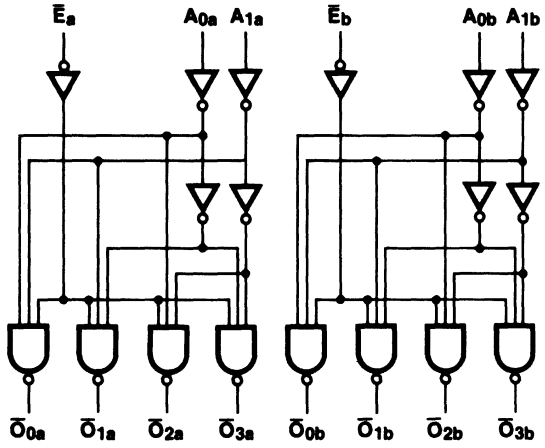
DIP
TOP VIEW



SSDFCT139-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDFCT139-003

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CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL	—	0.3	0.5	
			I_{OL} = 48mA COM	—	0.3	0.5	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 10 MHz Outputs Open One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	1.5	5.0	mA
			V_{IN} = 3.4V[4]	—	2.0	6.3	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V).
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V).

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
A_0, A_1	Address Inputs
$\overline{E}$	Enable Inputs (Active LOW)
$\overline{O}_0$-$\overline{O}_3$	Outputs (Active LOW)

TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A_0 or A_1 to $\overline{O}_n$	C_L = 50 pf R_L = 500Ω	6.0	3.0	9.0	2.5	12.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{O}_n$		5.5	3.0	8.0	2.5	9.0	ns

Integrated Device Technology Inc

FAST™ CMOS CARRY LOOKAHEAD GENERATOR

IDT54/74FCT182

FEATURES:

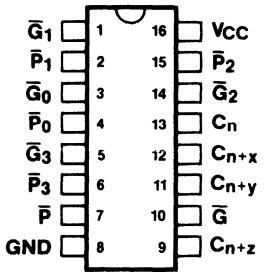
- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- 6ns typical propagation delay
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Carry lookahead generator
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT54/74FCT182 are high-speed carry lookahead generators built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The IDT54/74FCT182 are generally used with a 4-bit arithmetic logic unit to provide high-speed lookahead over word lengths of more than four bits.

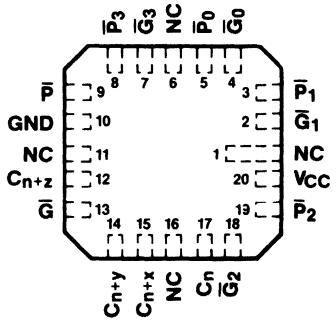
MEMORY INTERFACE

PIN CONFIGURATIONS



SSDFCT182-001

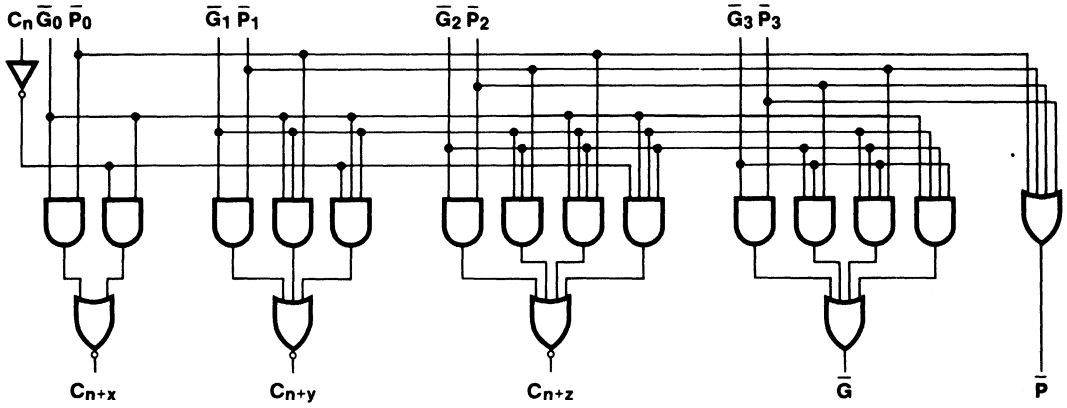
DIP
TOP VIEW



SSDFCT182-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDFCT182-003

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CEMOS is a trademark of Integrated Device Technology, Inc.

Printed in U.S.A.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL	—	0.3	0.5	
			I_{OL} = 48mA COM	—	0.3	0.5	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V(4)		—	0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	—	mA/ MHz
I_{CC}	Total Power Supply Current	V_{CC} = Max. f = 10 MHz Outputs Open One Input Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	1.5	—	mA
			V_{IN} = 3.4V(4)	—	2.0	—	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
C_n	Carry Input
$\overline{G}_0$, $\overline{G}_2$	Carry Generate Inputs (Active LOW)
$\overline{G}_1$	Carry Generate Input (Active LOW)
$\overline{G}_3$	Carry Generate Input (Active LOW)
$\overline{P}_0$, $\overline{P}_1$	Carry Propagate Inputs (Active LOW)
$\overline{P}_2$	Carry Propagate Input (Active LOW)
$\overline{P}_3$	Carry Propagate Input (Active LOW)
C_{n+x}-C_{n+z}	Carry Outputs
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)

TRUTH TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay C_N to C_{N+X}, C_{N+Y}, C_{N+Z}	C_L = 50 pf R_L = 500Ω	6.0	3.0	10.0	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_0$, $\overline{P}_1$, or $\overline{P}_2$, to C_{N+X}, C_{N+Y}, C_{N+Z}		6.0	2.0	9.0	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_0$, $\overline{G}_1$, or $\overline{G}_2$, to C_{N+X}, C_{N+Y}, C_{N+Z}		6.0	2.0	9.5	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_1$, $\overline{P}_2$, or $\overline{P}_3$, to $\overline{G}$		7.0	3.0	11.0	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_N$ to $\overline{G}$		7.5	3.0	11.5	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_N$ to $\overline{P}$		6.0	2.5	8.5	—	—	ns

Integrated Device Technology Inc

FAST™ CMOS OCTAL BUFFER/LINE DRIVER

IDT54/74FCT240

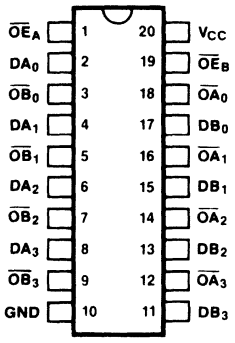
FEATURES:

- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- 5ns typical data to output delay
- I_{OL} = 48mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal buffer/line driver with 3-state output
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

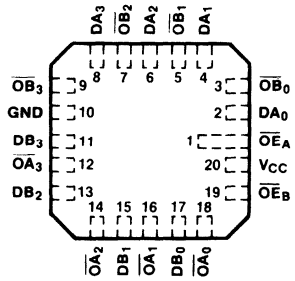
The IDT54/74FCT240 are octal buffer/line drivers built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The devices are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved board density.

PIN CONFIGURATIONS



SSDFCT240-001

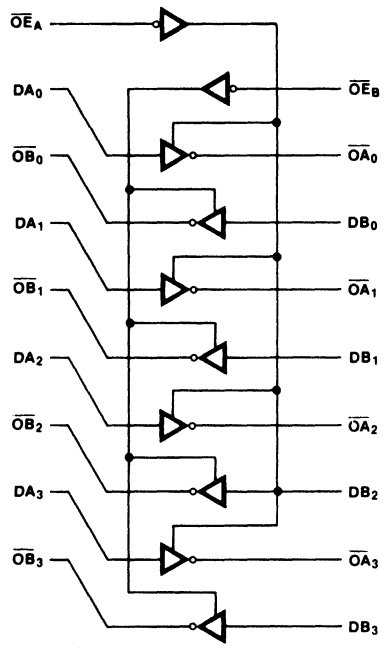
DIP
TOP VIEW



SSDFCT240-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDFCT240-003

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	μA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32μA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300μA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	—	GND	V_{LC}	
			I_{OL} = 48mA MIL	—	0.3	0.55	
			I_{OL} = 64mA COM	—	0.3	0.55	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-40	µA
			V_O = 2.4V	—	—	40	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN} \le V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}_N$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 10 MHz Outputs Open $\overline{OE}_N$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	1.5	5.0	mA
			V_{IN} = 3.4V[4]	—	2.0	6.3	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Input (Active LOW)
Dxx	Inputs
$\overline{O}$xx	Outputs

TRUTH TABLE

INPUTS		OUTPUT
$\overline{OE}_A$, $\overline{OE}_B$	D	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_N to $\overline{O}_N$	C_L = 50pf R_L = 500Ω	5.0	2.0	8.0	2.0	9.0	ns
t_{ZH} t_{ZL}	Output Enable Time		7.0	2.0	10.0	2.0	10.5	ns
t_{HZ} t_{LZ}	Output Disable Time		6.0	2.0	9.5	2.0	12.5	ns

FAST™ CMOS OCTAL BUFFER/LINE DRIVER

IDT54/74FCT244

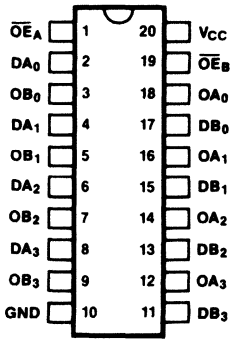
FEATURES:

- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- 4.5ns typical data to output delay
- I_{OL} = 48mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal buffer/line driver with 3-state output
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

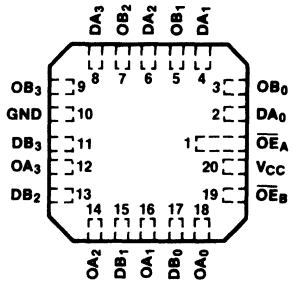
The IDT54/74FCT244 are octal buffer/line drivers built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The devices are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC and board density.

PIN CONFIGURATIONS



SSDFCT244-001

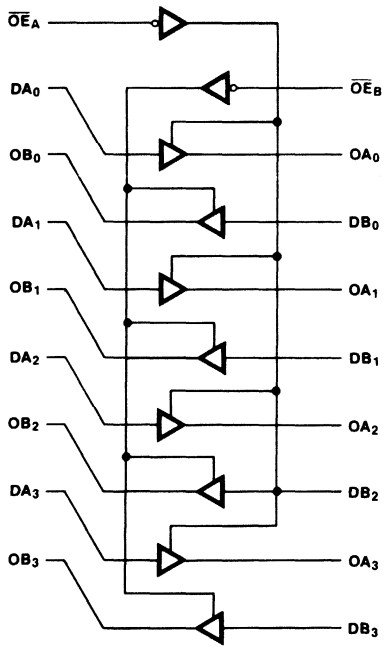
DIP
TOP VIEW



SSDFCT244-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDFCT244-003

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	μA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32μA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300μA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	—	GND	V_{LC}	
			I_{OL} = 48mA MIL	—	0.3	0.55	
			I_{OL} = 64mA COM	—	0.3	0.55	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-40	µA
			V_O = 2.4V	—	—	40	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN} \le V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 10 MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	1.5	5.0	mA
			V_{IN} = 3.4V[4]	—	2.0	6.3	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Input (Active LOW)
Dxx	Inputs
Oxx	Outputs

TRUTH TABLE

INPUTS		OUTPUT
$\overline{OE}_A$, $\overline{OE}_B$	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50pf R_L = 500Ω	4.5	2.5	6.5	2.0	7.0	ns
t_{ZH} t_{ZL}	Output Enable Time		6.0	2.0	8.0	2.0	8.5	ns
t_{HZ} t_{LZ}	Output Disable Time		5.0	2.0	7.0	2.0	7.5	ns

FAST™ CMOS NON-INVERTING BUFFER TRANSCEIVER

IDT54/74FCT245

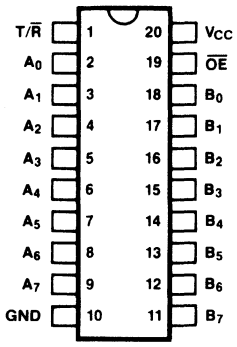
FEATURES:

- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- 5.0ns typical clock to output delay
- I_{OL} = 32mA port A, 48mA port B over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Non-inverting buffer transceiver
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

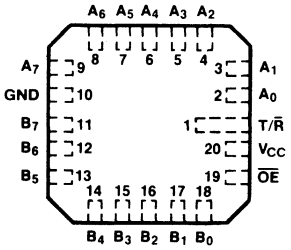
The IDT54/74FCT245 are 8-bit non-inverting, bidirectional buffers built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. This bidirectional buffer has 3-state outputs and is intended for bus-oriented applications. The Transmit/Receive (T/$\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports. Receive (active LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in High Z condition.

PIN CONFIGURATIONS



DIP
TOP VIEW

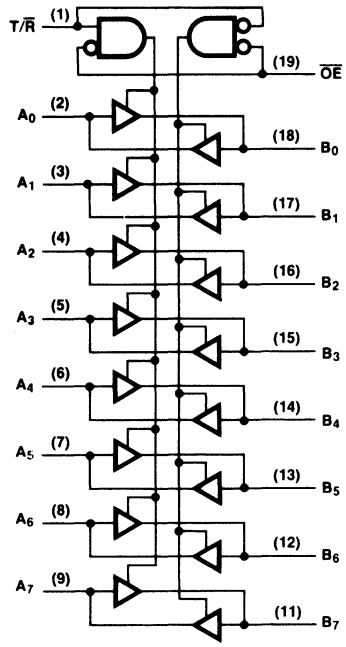
SSDFCT245-001



LCC
TOP VIEW

SSDFCT245-002

FUNCTIONAL BLOCK DIAGRAM



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MILITARY AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage Ports A and B	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage Port A	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL	—	0.3	0.5	
			I_{OL} = 48mA COM	—	0.3	0.5	
V_{OL}	Output LOW Voltage Port B	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC} I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 48mA MIL	—	0.3	0.55	
			I_{OL} = 64mA COM	—	0.3	0.55	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-45	µA
			V_O = 2.4V	—	—	45	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 10 MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	1.5	4.5	mA
			V_{IN} = 3.4V[4]	—	2.0	5.8	
$V_+ - V_-$	Hysteresis	$\overline{OE}$ and All Data Inputs		—	0.2	—	V

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V).
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V).

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_0	Side B Inputs or 3-State Outputs

TRUTH TABLE

INPUTS		OUTPUT
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B B to A	C_L = 50 pF R_L = 500 Ω	5.0	2.5	7.0	2.0	7.5	ns
t_{ZH} t_{ZL}	Output Enable Time		6.0	3.0	9.5	3.0	10.0	ns
t_{HZ} t_{LZ}	Output Disable Time		6.0	2.0	7.5	2.5	10.0	ns
t_{DLH} t_{DHL}	Propagation Delay T/$\overline{R}$ to A or B*		12.0	—	—	—	—	ns

*Guaranteed by design

FAST™ CMOS OCTAL D FLIP-FLOP WITH CLEAR

IDT54/74FCT273

Integrated Device Technology, Inc.

FEATURES:

- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- 7ns typical clock to output
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal D flip-flop with clear
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

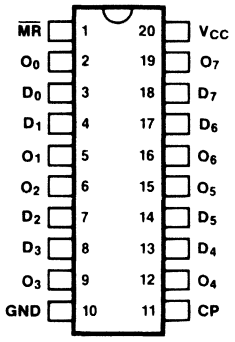
DESCRIPTION:

The IDT54/74FCT273 are octal D flip-flops built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The IDT54/74FCT273 have eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output.

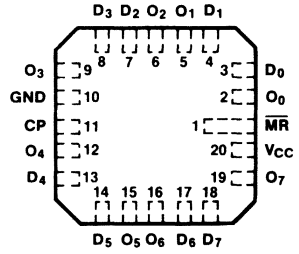
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

PIN CONFIGURATIONS



SSDAHCT273-001

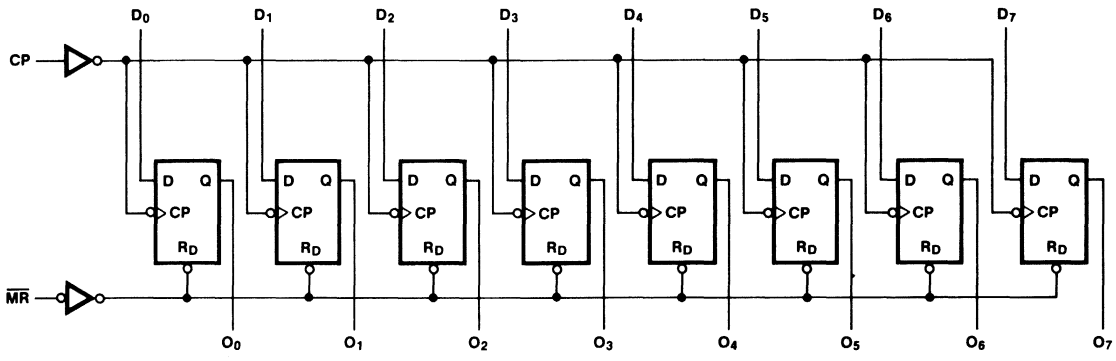
DIP
TOP VIEW



SSDAHCT273-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDAHCT273-003

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CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL	—	—	0.4	
			I_{OL} = 48mA COM	—	—	0.5	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 10 MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	1.5	5.0	mA
			V_{IN} = 3.4V[4]	—	2.0	7.5	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f/2 \times N) + (I_{CCQT} \times D \times N_D)$
   N = Number of total inputs toggling.
   f = Clock or latch enable frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
$\overline{MR}$	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
O_0-O_7	Data Outputs

TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUT
	$\overline{MR}$	CP	D_N	O_N
Reset (Clear)	L	X	X	L
Load "1"	H	⌐↑	h	H
Load "0"	H	⌐↑	l	L

H = HIGH Voltage Level steady state
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level steady state
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = DON'T CARE
⌐↑ = LOW to HIGH clock transition

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	C_L = 50 pf R_L = 500Ω	7.0	—	—	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to Output		8.0	—	—	—	—	ns
t_S	Set Up Time HIGH or LOW Data to CP		3.0	—	—	—	—	ns
t_H	Hold Time HIGH or LOW Data to CP		1.0	—	—	—	—	ns
t_W	Clock Pulse Width HIGH or LOW		4.0	—	—	—	—	ns
t_{REC}	Recovery Time $\overline{MR}$ to CP		3.0	—	—	—	—	ns

FAST™ CMOS 8-INPUT UNIVERSAL SHIFT REGISTER

IDT54/74FCT299

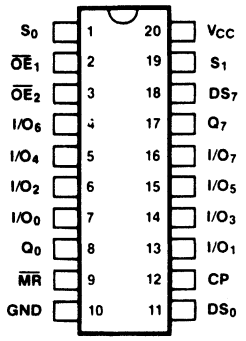
FEATURES:

- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- 7ns typical clock to output
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- 8-input universal shift register
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

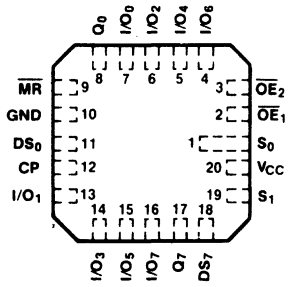
The IDT54/74FCT299 are 8-bit universal shift registers built using advanced CEMOS™ II, a dual metal 1.5 μm CMOS technology. The IDT54/74FCT299 are 8-bit universal shift/storage registers with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0-Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

PIN CONFIGURATIONS



SSDFCT299-001

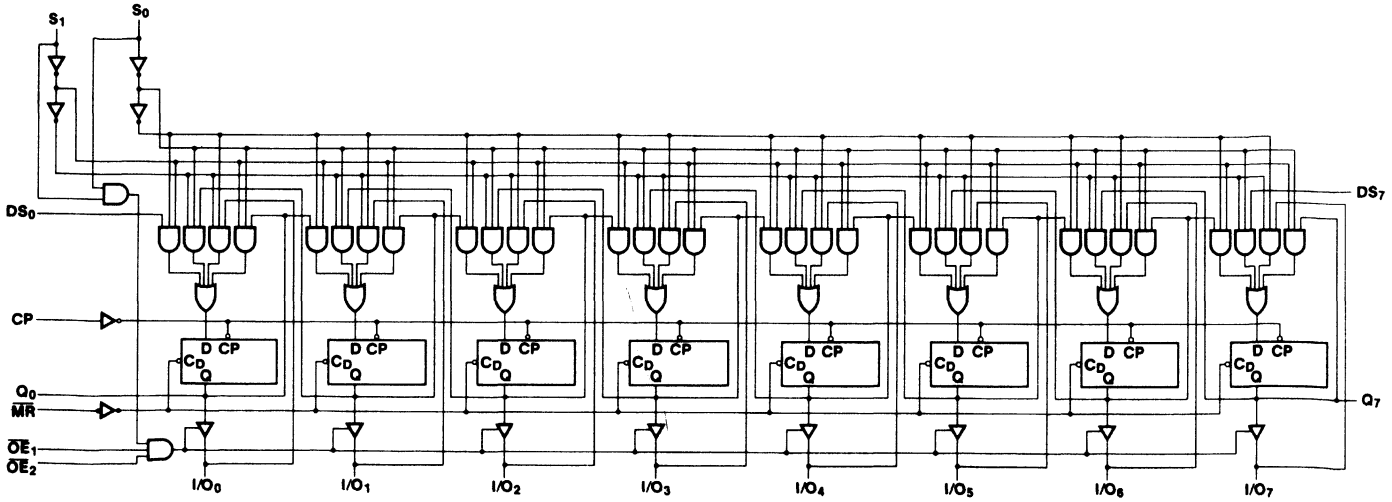
DIP
TOP VIEW



SSDFCT299-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDFCT299-003

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL	—	0.3	0.5	
			I_{OL} = 48mA COM	—	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-40	µA
			V_O = 2.4V	—	—	40	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V(4)		—	0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15		mA/ MHz

MEMORY INTERFACE

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 10 MHz $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	1.5		mA
			V_{IN} = 3.4V[4]	—	2.0		
$V_+ - V_-$	Hysteresis	CP and $\overline{OE}_N$		—	0.2	—	V

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f/2 \times N) + (I_{CCOT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Clock or latch enable frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
CP	Clock Pulse Input (Active Rising Edge)
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)
I/O_0-I/O_7	Parallel Data Inputs or 3-State Parallel Inputs
Q_0, Q_7	Serial Outputs

TRUTH TABLE

INPUTS				RESPONSE
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; Q_0-Q_7 = LOW
H	H	H	↑	Parallel Load; $I/O_N \rightarrow Q_N$
H	L	H	↑	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	↑	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH transition

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	C_L = 50pf R_L = 500Ω	7.0	3.5	10.0	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_N		6.0	4.0	12.0	—	—	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7		7.0	4.5	10.5	—	—	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_N		7.0	6.5	15.0	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_N		8.0	3.5	11.0	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_N		5.5	2.0	7.0	—	—	ns
t_S	Setup Time HIGH or LOW S_0 or S_1 to CP		2.0	8.5	—	—	—	ns
t_H	Hold Time HIGH or LOW S_0 or S_1 to CP		0	0	—	—	—	ns
t_S	Setup Time HIGH or LOW I/O_N, DS_0 or DS_7 to CP		0.5	5.5	—	—	—	ns
t_H	Hold Time HIGH or LOW I/O_N, DS_0 or DS_7 to CP		0	2.0	—	—	—	ns
t_W	CP Pulse Width HIGH or LOW		7.0	7.0	—	—	—	ns
t_W	$\overline{MR}$ Pulse Width LOW		7.0	7.0	—	—	—	ns
t_{REC}	Recovery Time $\overline{MR}$ to CP		7.0	7.0	—	—	—	ns

Integrated Device Technology, Inc.

FAST™ CMOS OCTAL TRANSPARENT LATCH

IDT54/74FCT373

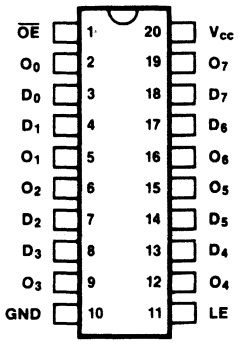
FEATURES:

- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- 5ns typical data to output delay
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal transparent latch with enable
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

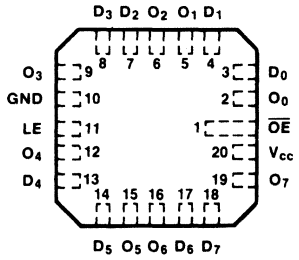
The IDT54/74FCT373 are 8-bit latches built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. This octal latch has 3-state outputs and is intended for bus-oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

PIN CONFIGURATIONS



SSDFCT373-001

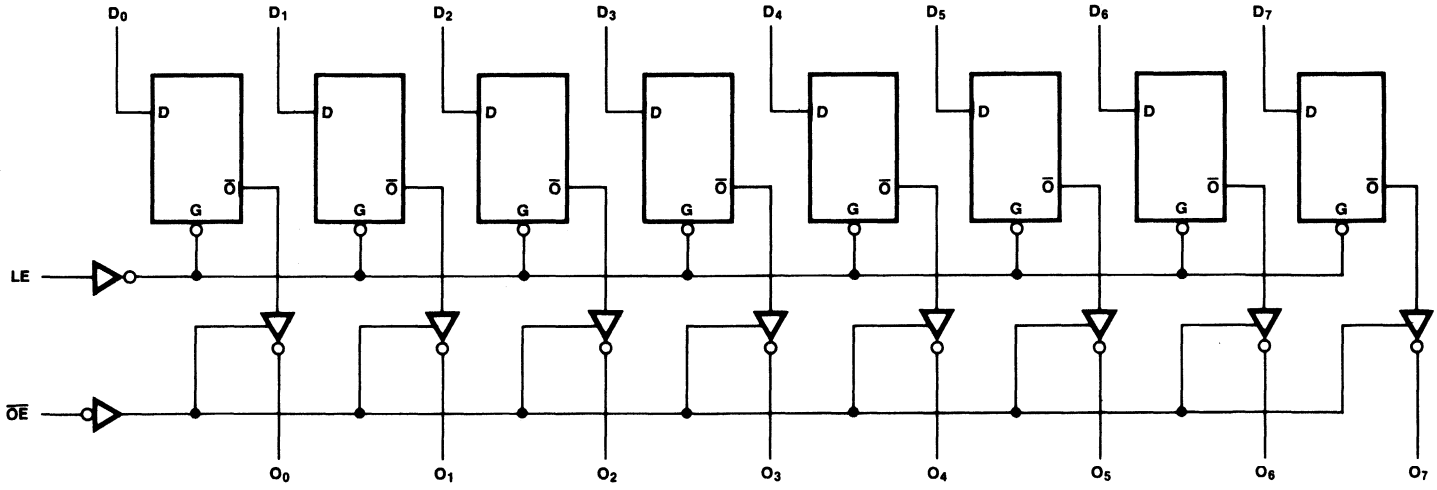
DIP
TOP VIEW



SSDFCT373-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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SSDFCT373-003

MEMORY INTERFACE

MILITARY AND COMMERCIAL TEMPERATURE RANGES

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Input Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL	—	0.3	0.5	
			I_{OL} = 48mA COM	—	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-40	µA
			V_O = 2.4V	—	—	40	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN} \le V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 10 MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	1.5	4.5	mA
			V_{IN} = 3.4V[4]	—	2.0	7.0	
$V_+ - V_-$	Hysteresis	LE and $\overline{OE}$ Inputs Only		—	0.2	—	V

NOTES

(1) For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.

(2) Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

(3) Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

(4) Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

(5) $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f/_2 \times N) + (I_{CCQT} \times D \times N_D)$
N = Total number of inputs toggling.
f = Clock or latch enable frequency in MHz.
D = Percent high duty cycle.
N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V).
N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V).

TRUTH TABLE

INPUTS		OUTPUTS	
D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
O_0-O_7	3-State Latch Outputs

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	C_L = 50 pf R_L = 500 Ω	5.0	2.0	8.0	2.0	8.5	ns
t_{ZH} t_{ZL}	Output Enable Time		7.0	2.0	12.0	2.0	13.5	ns
t_{HZ} t_{LZ}	Output Disable Time		6.0	2.0	7.5	2.0	10.0	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_n		9.0	3.0	13.0	3.0	15.0	ns
t_S	Set up Time High or Low D_n to LE		1.0	2.0	—	2.0	—	ns
t_H	Hold Time High or Low D_n to LE		1.0	3.0	—	3.0	—	ns
t_W	LE Pulse Width High or Low		5.0	6.0	—	6.0	—	ns

FAST™ CMOS OCTAL D REGISTER (3-STATE)

IDT54/74FCT374

FEATURES:

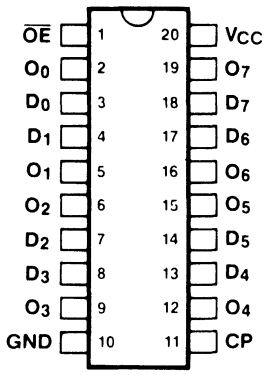
- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- 7.5ns typical clock to output delay
- I_{OL} = 32 mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST (5μA max.)
- Positive, edge-triggered master/slave, D-type flip-flops
- Buffered common clock and buffered common three-state control
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT54/74FCT374 are 8-bit registers built using advanced CEMOS™II, a dual metal 1.5μm CMOS technology. This register consists of eight D-type flip-flops with a buffered common clock and buffered three-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the three-state conditions.

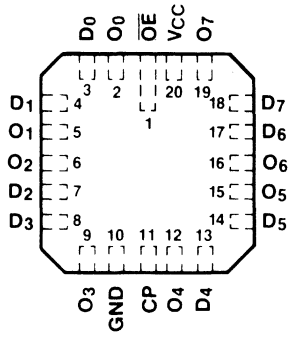
Input data meeting the set-up and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

PIN CONFIGURATIONS



SSDAHCT374-001

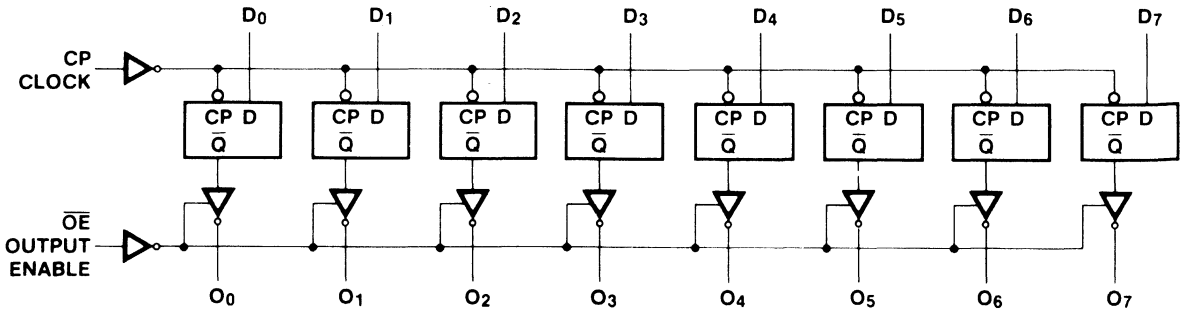
DIP
TOP VIEW



SSDAHCT374-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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MILITARY AND COMMERCIAL TEMPERATURE RANGES

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL	—	0.3	0.5	
			I_{OL} = 48mA COM	—	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-40	µA
			V_O = 2.4V	—	—	40	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 10 MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	1.5	4.5	mA
			V_{IN} = 3.4V[4]	—	2.0	7.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f/2 \times N) + (I_{CCQT} \times D \times N_D)$
   N = Number of total inputs toggling.
   f = Clock or latch enable frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	3-State Output Enable Input (Active LOW)
O_0-O_7	Complementary 3-State Outputs

TRUTH TABLE

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	$\overline{OE}$	CP	D_I	O_N	O_I
Hi-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L	↗	L	H	H
	L	↗	H	L	L
	H	↗	L	Z	H
	H	↗	H	Z	L

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
↗ = LOW-to-HIGH transition
NC = No Change

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_N	C_L = 50 pf R_L = 500Ω	6.5	4.0	10.0	4.0	11.0	ns
t_{ZH} t_{ZL}	Output Enable Time		9.0	2.0	12.5	2.0	14.0	ns
t_{HZ} t_{LZ}	Output Disable Time		6.0	2.0	8.0	2.0	8.0	ns
t_S	Set Up Time HIGH or LOW D_N to CP		1.0	2.0	—	2.5	—	ns
t_H	Hold Time HIGH or LOW D_N to CP		0.5	2.0	—	2.5	—	ns
t_W	CP Pulse Width HIGH or LOW		4.0	7.0	—	7.0	—	ns

FAST™ CMOS OCTAL D FLIP-FLOP WITH CLOCK ENABLE

IDT54/74FCT377

Integrated Device Technology, Inc.

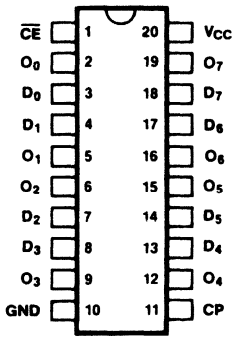
FEATURES:

- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- 7ns typical clock to output
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal D flip-flop with clock enable
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

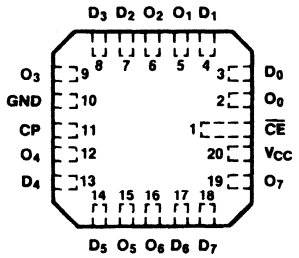
The IDT54/74FCT377 are octal D flip-flops built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The IDT54/74FCT377 have eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is LOW. The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

PIN CONFIGURATIONS



SSDFCT377-001

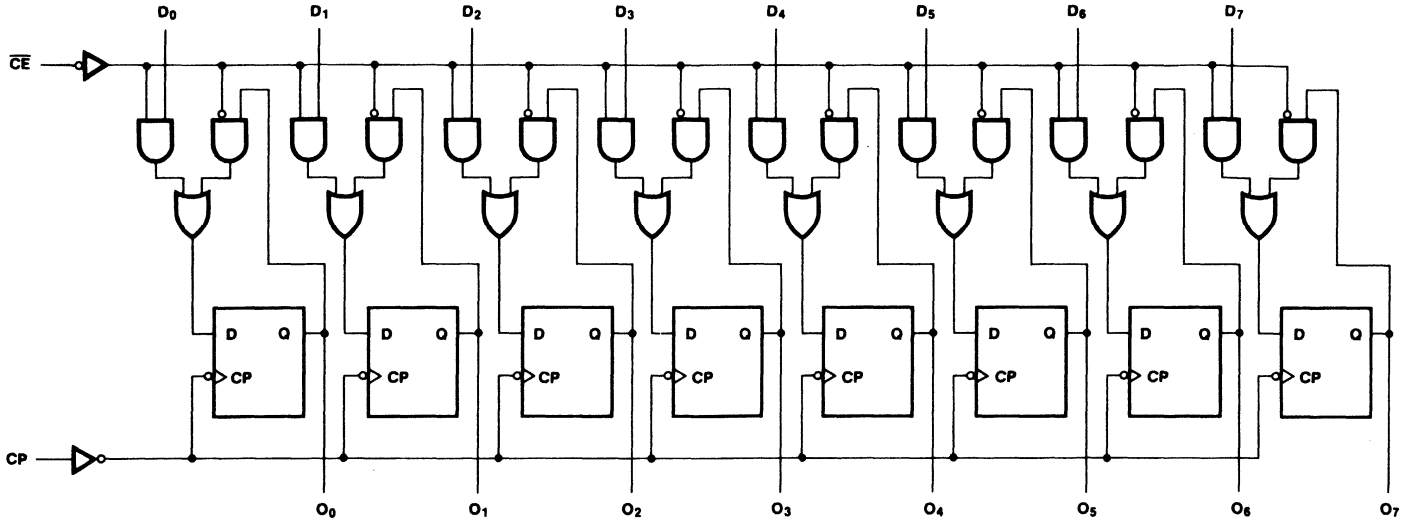
DIP
TOP VIEW



SSDFCT377-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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MEMORY INTERFACE

MILITARY AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	--	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL	—	0.3	0.5	
			I_{OL} = 48mA COM	—	0.3	0.5	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 10 MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	1.5	5.0	mA
			V_{IN} = 3.4V[4]	—	2.0	7.5	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f/2 \times N) + (I_{CCQT} \times D \times N_D)$
   N = Number of total inputs toggling.
   f = Clock or latch enable frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
O_0-O_7	Data Outputs
CP	Clock Pulse Input

TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{CE}$	D_N	O_N
Load "1"	⎍	l	h	H
Load "0"	⎍	l	l	L
Hold (Do Nothing)	⎍	h	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Don't care
⎍ = LOW-to-HIGH Clock Transition

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_N	C_L = 50 pf R_L = 500 Ω	7.0	—	—	—	—	ns
t_S	Set Up Time HIGH or LOW D_N to CP		3.0	—	—	—	—	ns
t_H	Hold Time HIGH or LOW D_N to CP		1.0	—	—	—	—	ns
t_S	Set Up Time HIGH or LOW $\overline{CE}$ to CP		3.0	—	—	—	—	ns
t_H	Hold Time HIGH or LOW $\overline{CE}$ to CP		1.0	—	—	—	—	ns
t_W	Clock Pulse Width, LOW		4.0	—	—	—	—	ns

Integrated Device Technology, Inc.

FAST™ CMOS 8-BIT IDENTITY COMPARATOR

IDT54/74FCT521

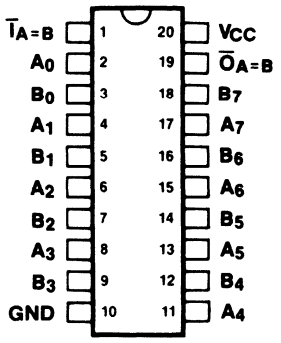
FEATURES:

- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- 7ns typical propagation delay
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- 8-bit identity comparator
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

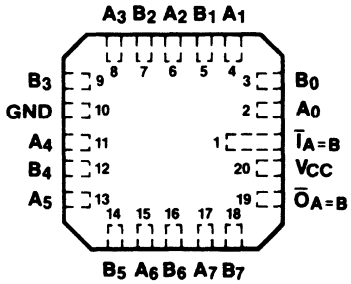
The IDT54/74FCT521 are 8-bit identity comparators built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The device compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

PIN CONFIGURATIONS



SSDFCT521-001

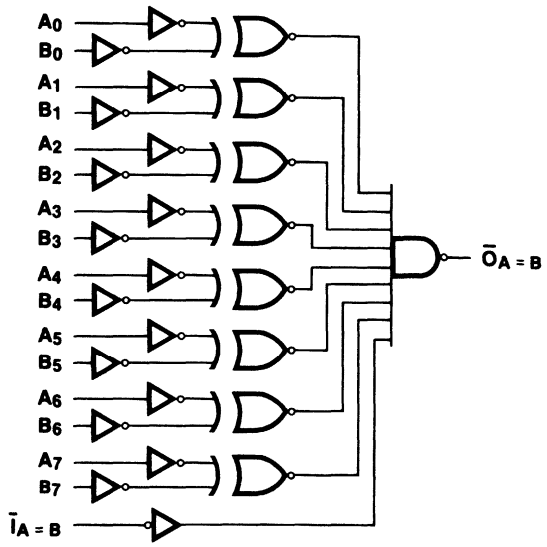
DIP
TOP VIEW



SSDFCT521-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDFCT521-003

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL	—	0.3	0.5	
			I_{OL} = 48mA COM	—	0.3	0.5	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	—	mA/ MHz
I_{CC}	Total Power Supply Current	V_{CC} = Max. f = 10 MHz Outputs Open One Input Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	1.5	—	mA
			V_{IN} = 3.4V[4]	—	2.0	—	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
A_0-A_7	Word A inputs
B_0-B_7	Word B inputs
$\overline{I}_{A=B}$	Expansion or Enable Input (Active LOW)
$\overline{O}_{A=B}$	Identity Output (Active Low)

TRUTH TABLE

INPUTS		OUTPUT
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A_N or B_N to $\overline{O}_{A=B}$	C_L = 50 pf R_L = 500 Ω	7.0	3.5	11.0	3.5	15.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$		5.0	3.0	10.0	3.0	9.0	ns

FAST™ CMOS OCTAL TRANSPARENT LATCH (3-STATE)

IDT54/74FCT533

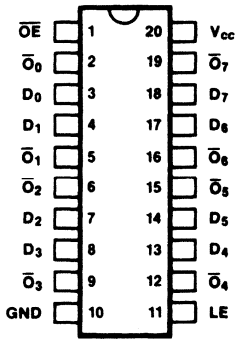
FEATURES:

- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- 6ns typical clock to output
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal transparent latch with 3-state output
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

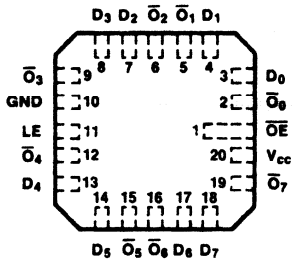
The IDT54/74FCT533 are octal transparent latches built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The IDT54/74FCT533 consist of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

PIN CONFIGURATIONS



SSDFCT533-001

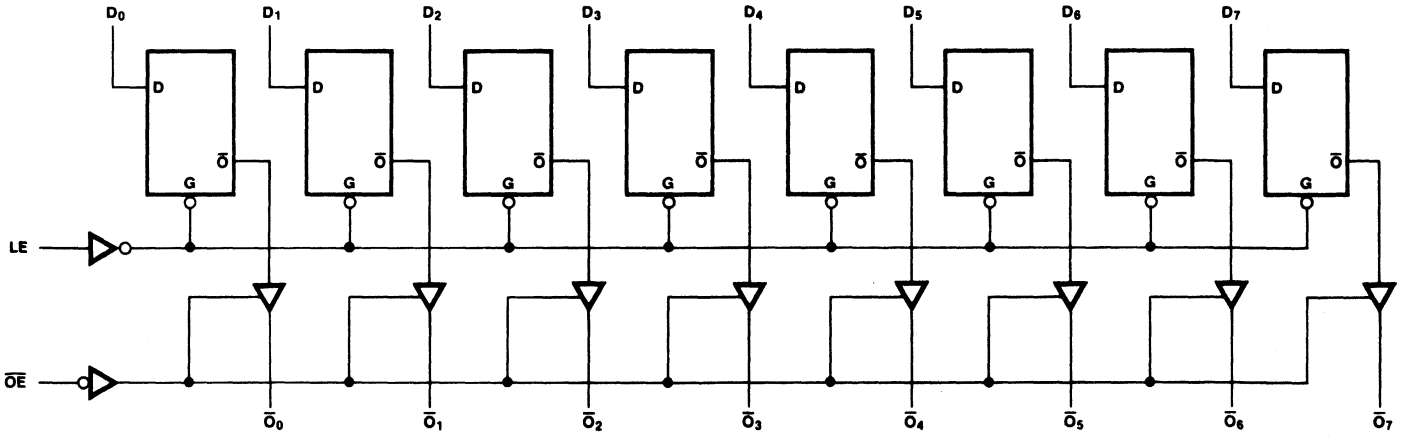
DIP
TOP VIEW



SSDFCT533-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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MILITARY, INDUSTRIAL, AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL	—	0.3	0.5	
			I_{OL} = 48mA COM	—	0.3	0.5	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-40	µA
			V_O = 2.4V	—	—	40	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 10 MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	1.5	5.0	mA
			V_{IN} = 3.4V[4]	—	2.0	7.5	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f/2 \times N) + (I_{CCQT} \times D \times N_D)$
   N = Number of total inputs toggling.
   f = Clock or latch enable frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
$\overline{LE}$	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{O}_0$-$\overline{O}_7$	Complementary 3-State Outputs

TRUTH TABLE

INPUTS		OUTPUTS	
D_N	LE	$\overline{OE}$	$\overline{O}_N$
H	H	L	L
L	H	L	H
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_N to $\overline{O}_N$	C_L = 50pf R_L = 500Ω	6.0	3.0	10.0	3.0	12.0	ns
t_{ZH} t_{ZL}	Output Enable Time		8.0	2.0	11.0	2.0	12.5	ns
t_{HZ} t_{LZ}	Output Disable Time		6.0	2.0	7.0	2.0	8.5	ns
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_N$		9.0	3.0	13.0	3.0	14.0	ns
t_S	Set Up Time HIGH or LOW D_N to LE		1.0	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW D_N to LE		0.5	3.0	—	3.0	—	ns
t_W	LE Pulse Width HIGH or LOW		5.0	6.0	—	6.0	—	ns

Integrated Device Technology, Inc.

FAST™ CMOS OCTAL D FLIP-FLOP (3-STATE)

IDT54/74FCT534

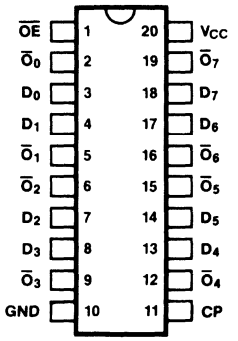
FEATURES:

- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- 6.5ns typical clock to output
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal D flip-flop with 3-state output
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

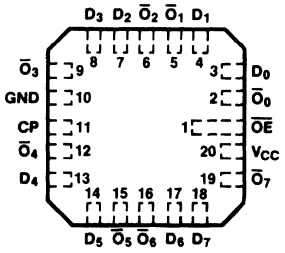
The IDT54/74FCT534 are octal D flip-flops built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The IDT54/74FCT534 are high-speed, low-power octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

PIN CONFIGURATIONS



SSDFCT534-001

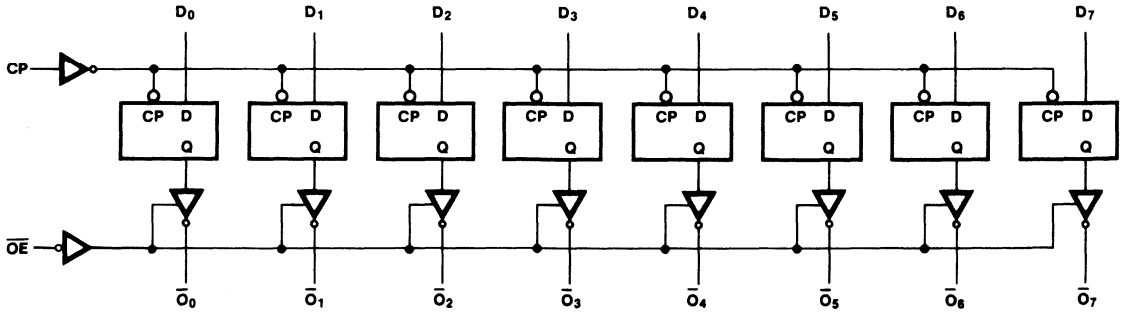
DIP
TOP VIEW



SSDFCT534-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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MILITARY AND COMMERCIAL TEMPERATURE RANGES

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL	—	0.3	0.5	
			I_{OL} = 48mA COM	—	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-40	µA
			V_O = 2.4V	—	—	40	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 10 MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	1.5	5.0	mA
			V_{IN} = 3.4V[4]	—	2.0	7.5	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f/2 \times N) + (I_{CCQT} \times D \times N_D)$
   N = Number of total inputs toggling.
   f = Clock or latch enable frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	3-State Output Enable Input (Active LOW)
$\overline{O}_0$-$\overline{O}_7$	Complementary 3-State Outputs

TRUTH TABLE

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	$\overline{OE}$	CP	D_I	$\overline{O}_N$	Q_I
Hi-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L	↑	L	H	H
	L	↑	H	L	L
	H	↑	L	Z	H
	H	↑	H	Z	L

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH transition
NC = No Change

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_N$	C_L = 50 pf R_L = 500Ω	6.5	4.0	10.0	4.0	11.0	ns
t_{ZH} t_{ZL}	Output Enable Time		9.0	2.0	12.5	2.0	14.0	ns
t_{HZ} t_{LZ}	Output Disable Time		6.0	2.0	8.0	2.0	8.0	ns
t_S	Set Up Time HIGH or LOW D_N to CP		1.0	2.0	—	2.5	—	ns
t_H	Hold Time HIGH or LOW D_N to CP		0.5	2.0	—	2.5	—	ns
t_W	CP Pulse Width HIGH or LOW		4.0	7.0	—	7.0	—	ns

FAST™ CMOS OCTAL INVERTING BUFFER TRANSCEIVER

IDT54/74FCT640

Integrated Device Technology, Inc.

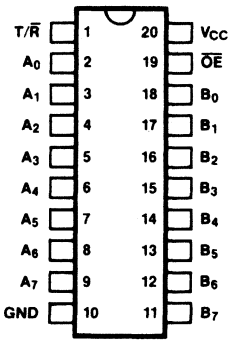
FEATURES:

- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- 6.0ns data to output
- I_{OL} = 48mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Inverting buffer transceiver
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

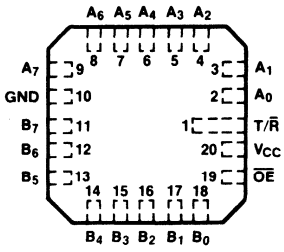
The IDT54/74FCT640 are 8-bit inverting buffer transceivers built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control ($T/\overline{R}$) input. The enable input ($\overline{OE}$) can be used to disable the device so the buses are effectively isolated.

PIN CONFIGURATIONS



SSDFCT640-001

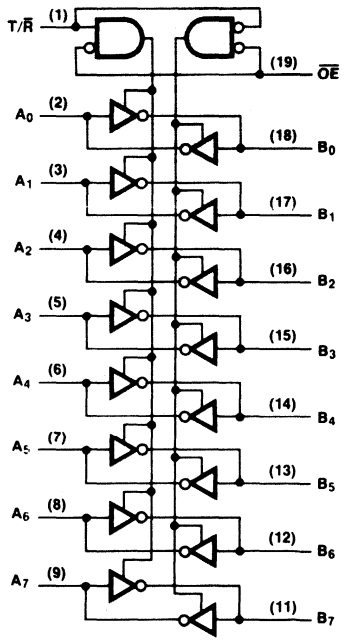
DIP
TOP VIEW



SSDFCT640-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDFCT640-003

MEMORY INTERFACE

FAST is a trademark of Fairchild Camera and Instrument.
CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 48mA MIL	—	0.3	0.55	
			I_{OL} = 64mA COM	—	0.3	0.55	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-45	µA
			V_O = 2.4V	—	—	45	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 10 MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	1.5	4.5	mA
			V_{IN} = 3.4V[4]	—	2.0	5.8	
$V_+ - V_-$	Hysteresis	$\overline{OE}$ and all Data Inputs		—	0.2	—	V

NOTES:

(1) For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.

(2) Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

(3) Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

(4) Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

(5) $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f \times N) + (I_{CCQT} \times D \times N_D)$

N = Total number of inputs toggling.
f = Frequency in MHz.
D = Percent high duty cycle.
N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V).
N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V).

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_7	Side B Inputs or 3-State Outputs

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A	C_L = 50 pf R_L = 500 Ω	6.0	2.0	7.0	2.0	8.0	ns
t_{ZH} t_{ZL}	Output Enable Time		7.0	2.0	10.0	2.0	12.0	ns
t_{HZ} t_{LZ}	Output Disable Time		11.0	2.0	13.0	2.0	16.0	ns
t_{DLH} t_{DHL}	Propagation Delay T/$\overline{R}$ to A or B*		12.0	—	—	—	—	ns

*Guaranteed by Design

MEMORY INTERFACE

Integrated Device Technology, Inc.

FAST™ CMOS NON-INVERTING BUFFER TRANSCEIVER

IDT54/74FCT645

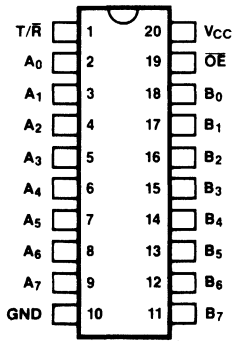
FEATURES:

- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- 6ns typical data to output
- I_{OL} = 48mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Non-inverting buffer transceiver
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

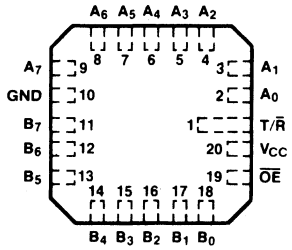
The IDT54/74FCT645 are 8-bit non-inverting buffer transceivers built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. These non-inverting buffer transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control (T/$\overline{R}$) input. The enable input ($\overline{OE}$) can be used to disable the device so the buses are effectively isolated.

PIN CONFIGURATIONS



SSDFCT645-001

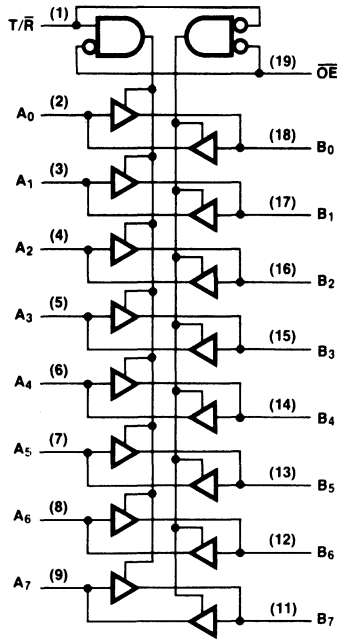
DIP
TOP VIEW



SSDFCT645-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDFCT645-003

FAST is a trademark of Fairchild Camera and Instrument.
CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level (Except I/O Pins)	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Input Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 48mA MIL	—	0.3	0.55	
			I_{OL} = 64mA COM	—	0.3	0.55	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-45	µA
			V_O = 2.4V	—	—	45	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 10 MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	1.5	4.5	mA
			V_{IN} = 3.4V[4]	—	2.0	5.8	
$V_+ - V_-$	Hysteresis	$\overline{OE}$ and all Data Inputs		—	0.2	—	V

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CC} \times f \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Clock or latch enable.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V).
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V).

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_7	Side B Inputs or 3-State Outputs

FUNCTION TABLE

INPUTS		OPERATIONS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A	C_L = 50 pf R_L = 500Ω	6.0	2.0	9.5	2.0	11.0	ns
t_{ZH} t_{ZL}	Output Enable Time		9.0	2.0	11.0	2.0	12.0	ns
t_{HZ} t_{LZ}	Output Disable Time		6.0	2.0	12.0	2.0	13.0	ns
t_{DLH} t_{DHL}	Propagation Delay T/$\overline{R}$ to A or B*		12.0	—	—	—	—	ns

*Guaranteed by Design

Integrated Device Technology Inc

HIGH-SPEED CMOS 1-of-8 DECODER

IDT54/74AHCT138

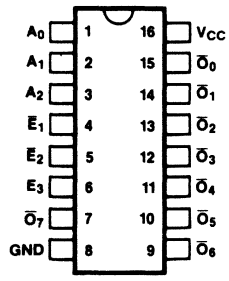
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 11ns typical address to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- 1-of-8 decoder with enables
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

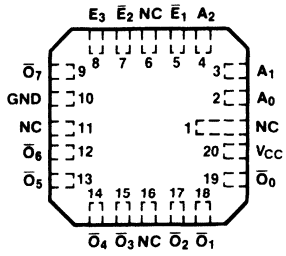
The IDT54/74AHCT138 are 1-of-8 decoders built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The IDT54/74AHCT138 accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The IDT54/74AHCT138 features three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four IDT54/74AHCT138 devices and one inverter.

PIN CONFIGURATIONS



SSDAHCT138-001

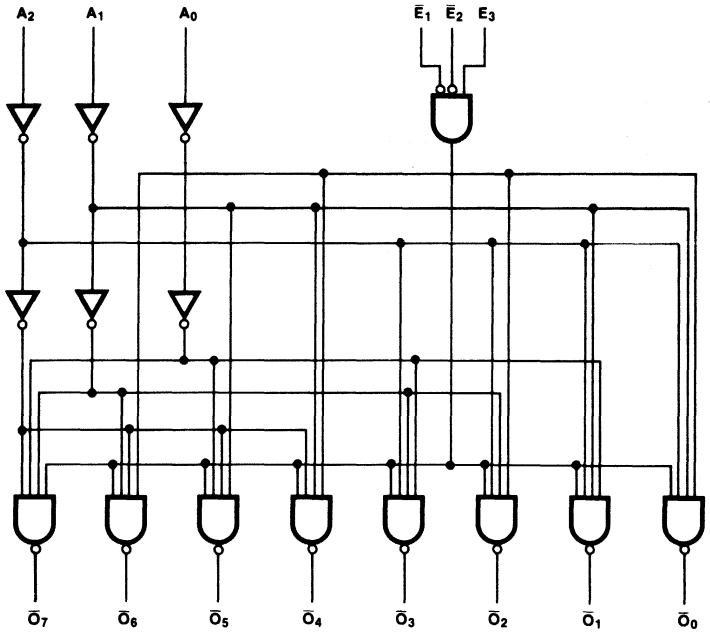
DIP
TOP VIEW



SSDAHCT138-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDAHCT138-003

MEMORY INTERFACE

CEMOS is a trademark of Integrated Device Technology, Inc.

Printed in U.S.A.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL	2.4	4.3	—	
			I_{OH} = -2.6mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN} \le V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 1 MHz Outputs Open One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	0.15	2.3	mA
			V_{IN} = 3.4V[4]	—	0.65	4.3	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V).
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V).

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
A_0-A_2	Address Inputs
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
$\overline{O}_0$-$\overline{O}_7$	Outputs (Active LOW)

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	O_0	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A_N to $\overline{O}_N$	C_L = 50 pf R_L = 500 Ω	11.0	6.0	22.0	6.0	27.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_N$		13.0	4.0	17.0	4.0	20.0	ns
t_{PLH} t_{PHL}	Propagation Delay E_3 to $\overline{O}_N$		13.0	4.0	17.0	4.0	20.0	ns

HIGH-SPEED CMOS DUAL 1-OF-4 DECODER

IDT54/74AHCT139

Integrated Device Technology Inc

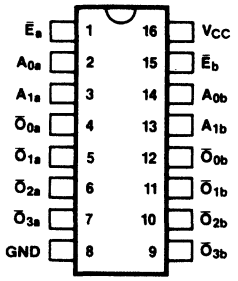
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 9ns typical address to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Dual 1-of-4 decoder with enable
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

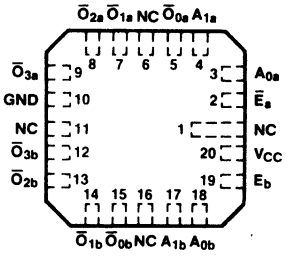
The IDT54/74AHCT139 are dual 1-of-4 decoders built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The device has two independent decoders, each of which accepts two binary weighted inputs (A_0-A_1) and provides four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH, all outputs are forced HIGH.

PIN CONFIGURATIONS



SSDAHCT139-001

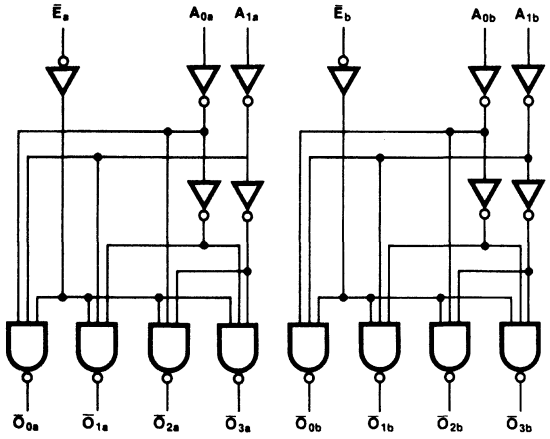
DIP
TOP VIEW



SSDAHCT139-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDAHCT139-003

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Input Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL	2.4	4.3	—	
			I_{OH} = -2.6mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN} \le V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 1 MHz Outputs Open One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	0.15	2.3	mA
			V_{IN} = 3.4V[4]	—	0.65	3.3	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Clock or latch enable.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V).
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V).

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
A_0, A_1	Address Inputs
$\overline{E}$	Enable Inputs (Active LOW)
$\overline{O}_0$-$\overline{O}_3$	Outputs (Active LOW)

TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A_0 or A_1 to $\overline{O}_N$	C_L = 50 pf R_L = 500 Ω	9.0	5.0	20.0	5.0	25.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{O}_N$		11.0	5.0	15.0	5.0	18.0	ns

HIGH-SPEED CMOS CARRY LOOKAHEAD GENERATOR

IDT54/74AHCT182

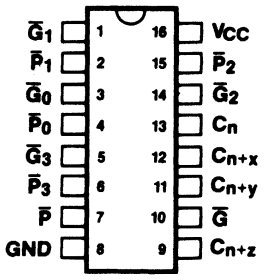
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 8ns typical propagation delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Carry lookahead generator
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

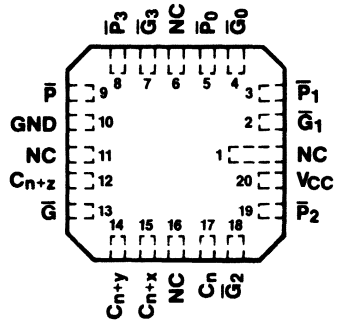
The IDT54/74AHCT182 are carry lookahead generators built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The IDT54/74AHCT182 are generally used with a 4-bit arithmetic logic unit to provide high-speed lookahead over word lengths of more than four bits.

PIN CONFIGURATIONS



SSDAHCT182-001

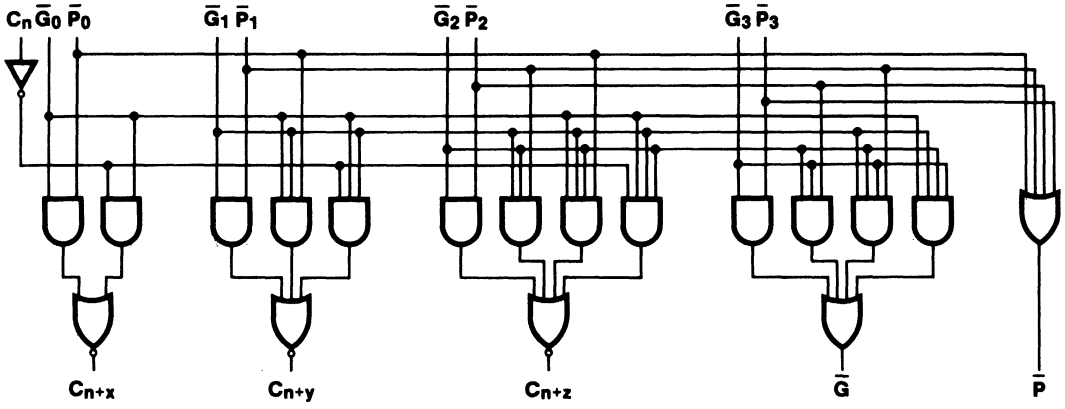
DIP
TOP VIEW



SSDAHCT182-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDAHCT182-003

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MEMORY INTERFACE

MILITARY AND COMMERCIAL TEMPERATURE RANGES

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -200µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V(4)		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	—	mA/ MHz
I_{CC}	Total Power Supply Current	V_{CC} = Max. f = 1 MHz Outputs Open One Input Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	—	mA
			V_{IN} = 3.4V(4)	—	0.65	—	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
C_n	Carry Input
$\overline{G}_0$, $\overline{G}_2$	Carry Generate Inputs (Active LOW)
$\overline{G}_1$	Carry Generate Input (Active LOW)
$\overline{G}_3$	Carry Generate Input (Active LOW)
$\overline{P}_0$, $\overline{P}_1$	Carry Propagate Inputs (Active LOW)
$\overline{P}_2$	Carry Propagate Input (Active LOW)
$\overline{P}_3$	Carry Propagate Input (Active LOW)
C_{n+x}-C_{n+z}	Carry Outputs
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)

TRUTH TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	H	H	X	H	H					L		
L	H	X	H	X	X	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	X	X	L	L				L	
	X		L	X	X	L	X	L				L	
	L		X		L	X	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		X		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay C_N to C_{N+X}, C_{N+Y}, C_{N+Z}	C_L = 50 pf R_L = 500Ω	8.0	—	—	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_0$, $\overline{P}_1$, or $\overline{P}_2$, to C_{N+X}, C_{N+Y}, C_{N+Z}		8.0	—	—	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_0$, $\overline{G}_1$, or $\overline{G}_2$, to C_{N+X}, C_{N+Y}, C_{N+Z}		8.0	—	—	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_1$, $\overline{P}_2$, or $\overline{P}_3$, to $\overline{G}$		9.0	—	—	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_N$ to $\overline{G}$		9.5	—	—	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_N$ to $\overline{P}$		8.0	—	—	—	—	ns

Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL BUFFER/LINE DRIVER

IDT54/74AHCT240

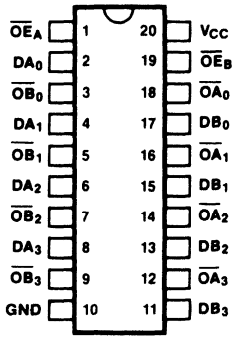
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 7ns typical data to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal buffer/line driver with 3-state output
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

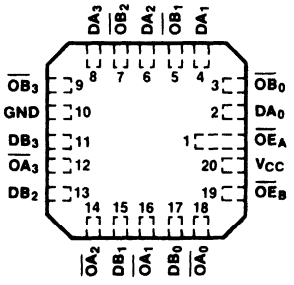
The IDT54/74AHCT240 are octal buffer/line drivers built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The devices are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved board density.

PIN CONFIGURATION



SSDAHCT240-001

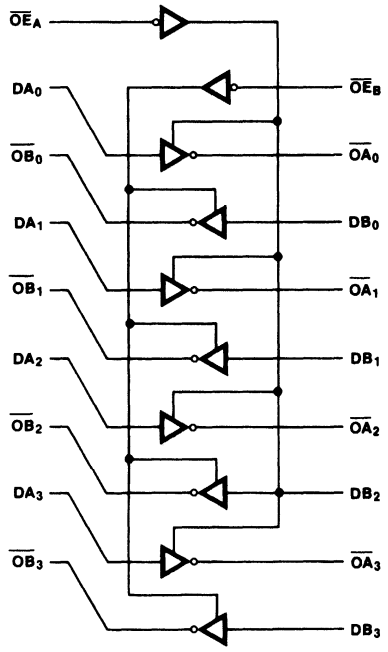
DIP
TOP VIEW



SSDAHCT240-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDAHCT240-003

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-10	µA
			V_O = 2.4V	—	—	10	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}_N$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 1 MHz Outputs Open $\overline{OE}_N$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	2.3	mA
			V_{IN} = 3.4V[4]	—	0.65	3.3	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Input (Active LOW)
Dxx	Inputs
Oxx	Outputs

TRUTH TABLE

INPUTS		OUTPUT
$\overline{OE}_A$, $\overline{OE}_B$	D	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_N to $\overline{O}_N$	C_L = 50pf R_L = 500Ω	7.0	2.0	9.0	2.0	12.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	5.0	18.0	5.0	20.0	ns
t_{HZ} t_{LZ}	Output Disable Time		10.0	2.0	12.0	2.0	18.0	ns

HIGH-SPEED CMOS OCTAL BUFFER/LINE DRIVER

IDT54/74AHCT244

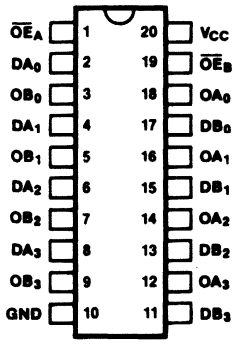
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 7ns typical data to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal buffer/line driver with 3-state output
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

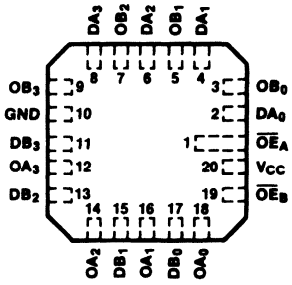
The IDT54/74AHCT244 are octal buffer/line drivers built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The devices are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved board density.

PIN CONFIGURATIONS



SSDAHCT244-001

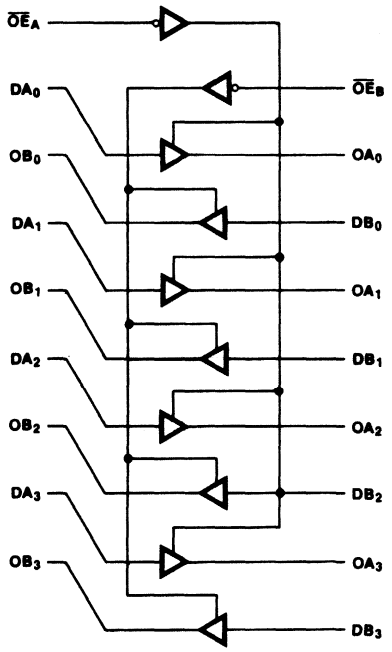
DIP
TOP VIEW



SSDAHCT244-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDAHCT244-003

MEMORY INTERFACE

CEMOS is a trademark of Integrated Device Technology, Inc.

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-10	µA
			V_O = 2.4V	—	—	10	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN} \le V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 1 MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	0.15	2.3	mA
			V_{IN} = 3.4V[4]	—	0.65	3.3	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Input (Active LOW)
Dxx	Inputs
Oxx	Outputs

TRUTH TABLE

INPUTS		OUTPUT
$\overline{OE}_A$, $\overline{OE}_B$	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50pf R_L = 500Ω	7.0	3.0	10.0	3.0	13.0	ns
t_{ZH} t_{ZL}	Output Enable Time		16.0	7.0	20.0	7.0	25.0	ns
t_{HZ} t_{LZ}	Output Disable Time		10.0	2.0	13.0	2.0	18.0	ns

HIGH-SPEED CMOS NON-INVERTING BUFFER TRANSCEIVER

IDT54/74AHCT245

Integrated Device Technology, Inc.

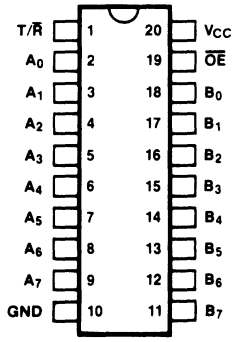
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 8ns typical data to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Non-inverting buffer transceiver
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

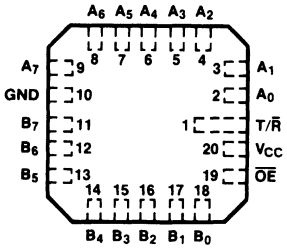
The IDT54/74AHCT245 are 8-bit non-inverting bidirectional buffers built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. This bidirectional buffer has 3-state outputs and is intended for bus-oriented applications. The Transmit/Receiver ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports. Receive (active LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

PIN CONFIGURATIONS



SSDAHCT245-001

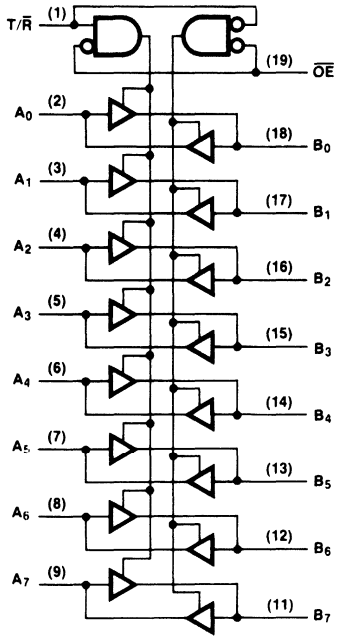
DIP
TOP VIEW



SSDAHCT245-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDAHCT245-003

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to + 70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to + 125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage Port A and B	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage Port A and B	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. I_{CC} = I_{CCQC} + (I_{CCQT} × N_T) × (I_{CCD} × f × N) + (I_{CCQT} × D × N_D)
   N = Total number of inputs toggling.
   f = Frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V).
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V).

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-15	µA
			V_O = 2.4V	—	—	15	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 1 MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	2.3	mA
			V_{IN} = 3.4V[4]	—	.65	3.3	
$V_+ - V_-$	Hysteresis	$\overline{OE}$ and all D Inputs		—	0.2	—	V

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) \times (I_{CCD} \times f \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V).
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V).

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_7	Side B Inputs or 3-State Outputs

TRUTH TABLE

INPUTS		OUTPUT
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B B to B	C_L = 50 pf R_L = 500Ω	8.0	3.0	10.0	3.0	15.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	5.0	20.0	5.0	25.0	ns
t_{HZ} t_{LZ}	Output Disable Time		11.0	2.0	15.0	2.0	18.0	ns
t_{DLH} t_{DHL}	Propagation Delay T/$\overline{R}$ to A or B*		14.0	—	—	—	—	ns

*Guaranteed by Design

HIGH-SPEED CMOS OCTAL D FLIP-FLOP WITH CLEAR

IDT54/74AHCT273

FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical clock to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal D flip-flop with clear
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

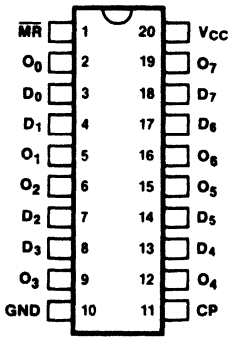
DESCRIPTION:

The IDT54/74AHCT273 are octal D flip-flops built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The IDT54/74AHCT273 has eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output.

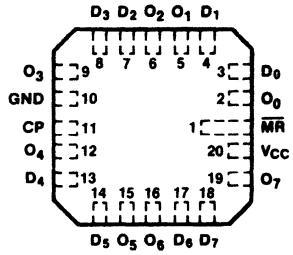
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

PIN CONFIGURATIONS



SSDAHCT273-001

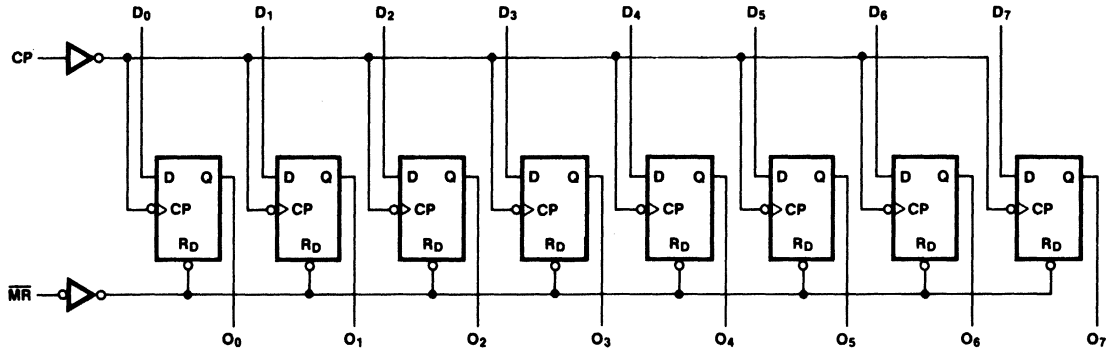
DIP
TOP VIEW



SSDAHCT273-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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MILITARY AND COMMERCIAL TEMPERATURE RANGES

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL	2.4	4.3	—	
			I_{OH} = -2.6mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 1MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	2.3	mA
			V_{IN} = 3.4V[4]	—	0.65	4.3	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f/2 \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Clock or latch enable frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
$\overline{MR}$	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
O_0-O_7	Data Outputs

TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUT
	$\overline{MR}$	CP	D_N	O_N
Reset (Clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

H = HIGH Voltage steady state
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
L = LOW Voltage Level steady state
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
X = Don't Care
↑ = LOW-to-HIGH clock transition

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_N	C_L = 50 pf R_L = 500Ω	10.0	3.0	15.0	3.0	17.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to Output		12.0	4.0	18.0	4.0	21.0	ns
t_S	Set Up Time High or Low Data to CP		3.0	10.0	—	10.0	—	ns
t_H	Hold Time High or Low Data to CP		0.6	1.0	—	1.0	—	ns
t_W	Clock Pulse Width High or Low		10.0	16.0	—	16.0	—	ns
t_{REC}	Recovery Time MR to CP		5.0	15.0	—	15.0	—	ns

HIGH-SPEED CMOS 8-INPUT UNIVERSAL SHIFT REGISTER

IDT54/74AHCT299

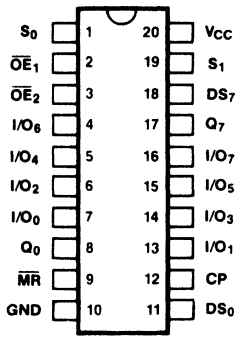
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 9ns typical clock to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- 8-input universal shift register
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

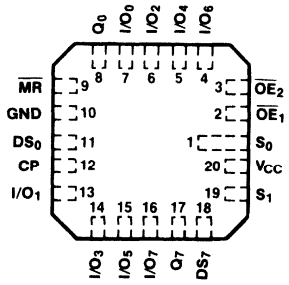
The IDT54/74AHCT299 are 8-bit universal shift registers built using advanced CEMOS™ II, a dual metal 1.5 μm CMOS technology. The IDT54/74AHCT299 are 8-bit universal shift/storage registers with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0-Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

PIN CONFIGURATIONS



SSDFCT299-001

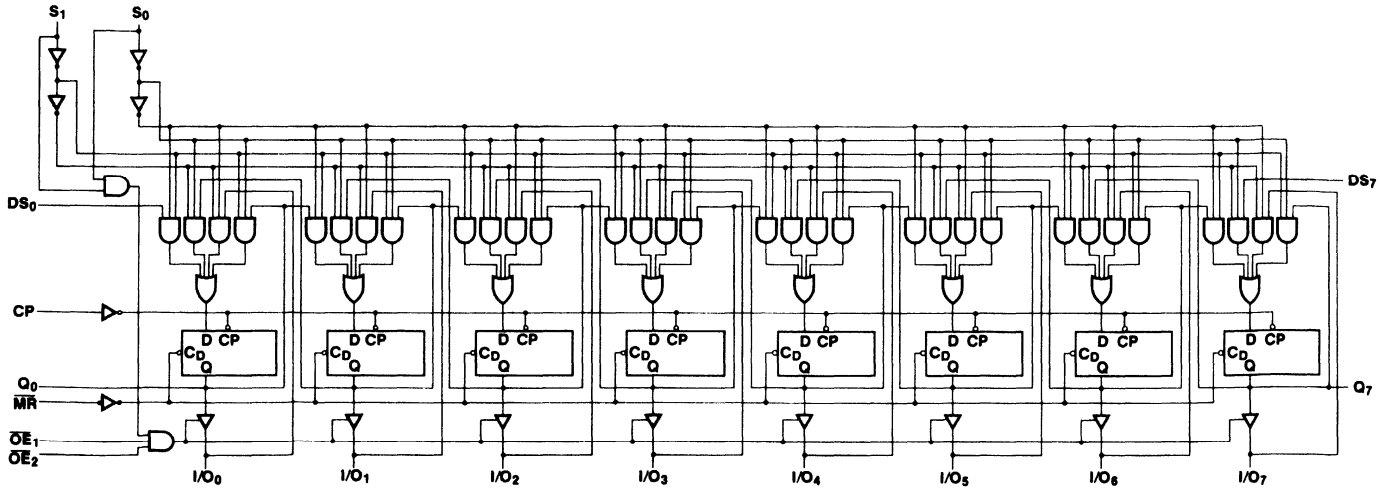
DIP
TOP VIEW



SSDFCT299-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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MILITARY AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -200µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-10	µA
			V_O = 2.4V	—	—	10	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V(4)		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	—	mA/ MHz

MEMORY INTERFACE

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 10 MHz Outputs Open $\overline{OE}_N$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	1.5		mA
			V_{IN} = 3.4V[4]	—	2.0		
$V_+ - V_-$	Hysteresis	CP and $\overline{OE}_N$		—	0.2	—	V

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f/2 \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
CP	Clock Pulse Input (Active Rising Edge)
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)
I/O_0-I/O_7	Parallel Data Inputs or 3-State Parallel Outputs
Q_0, Q_7	Serial Outputs

TRUTH TABLE

INPUTS				RESPONSE
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; Q_0-Q_7 = LOW
H	H	H	⎍	Parallel Load; $I/O_N \rightarrow Q_N$
H	L	H	⎍	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⎍	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⎍ = LOW-to-HIGH transition

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	C_L = 50 pf R_L = 500 Ω	9.0	—	—	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_N		8.0	—	—	—	—	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7		9.0	—	—	—	—	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_N		9.0	—	—	—	—	ns
t_{ZH} t_{ZL}	Output Enable Time $\overline{OE}$ to I/O_N		10.0	—	—	—	—	ns
t_{HZ} t_{LZ}	Output Disable Time $\overline{OE}$ to I/O_N		7.5	—	—	—	—	ns
t_S	Setup Time HIGH or LOW S_0 or S_1 to CP		4.0	—	—	—	—	ns
t_H	Hold Time HIGH or LOW S_0 or S_1 to CP		1.0	—	—	—	—	ns
t_S	Setup Time HIGH or LOW I/O_N, DS_0 or DS_7 to CP		1.5	—	—	—	—	ns
t_H	Hold Time HIGH or LOW I/O_N, DS_0 or DS_7 to CP		0	—	—	—	—	ns
t_W	CP Pulse Width HIGH or LOW		8.0	—	—	—	—	ns
t_W	$\overline{MR}$ Pulse Width Low		8.0	—	—	—	—	ns
t_{REC}	Recovery Time $\overline{MR}$ to CP		8.0	—	—	—	—	ns

HIGH-SPEED CMOS OCTAL TRANSPARENT LATCH

IDT54/74AHCT373

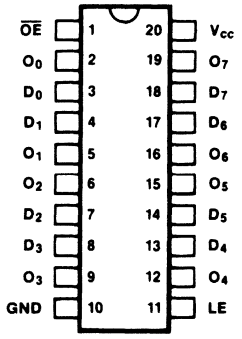
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical data to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal transparent latch with enable
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

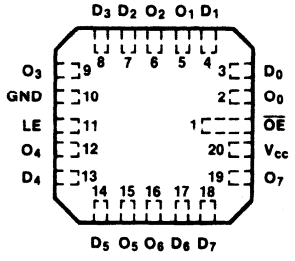
The IDT54/74AHCT373 are 8-bit latches built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. This octal latch has 3-state output and is intended for bus-oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

PIN CONFIGURATIONS



SSDAHCT373-001

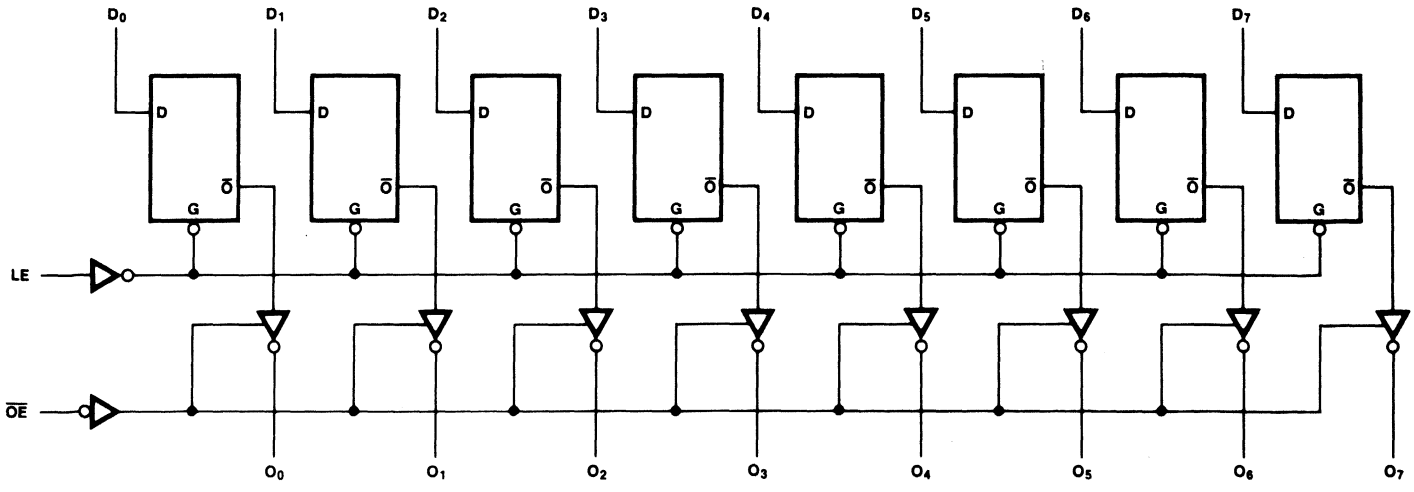
DIP
TOP VIEW



SSDAHCT373-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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MEMORY INTERFACE

MILITARY AND COMMERCIAL TEMPERATURE RANGES

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL	2.4	4.3	—	
			I_{OH} = -2.6mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-10	µA
			V_O = 2.4V	—	—	10	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN} \le V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 1 MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	0.15	2.3	mA
			V_{IN} = 3.4V[4]	—	0.65	4.3	
$V_+ - V_-$	Hysteresis	LE and $\overline{OE}$ Inputs		—	0.2	—	V

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f/2 \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Clock or latch enable frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V).
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V).

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
$\underline{LE}$	Latch Enables Input (Active HIGH)
$\overline{OE}$	Output Enables Input (Active LOW)
O_0-O_7	3-State Latch Outputs

TRUTH TABLE

INPUTS		OUTPUTS	
D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50 pf R_L = 500Ω	10.0	2.0	16.0	2.0	19.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	5.0	20.0	5.0	24.0	ns
t_{HZ} t_{LZ}	Output Disable Time		9.0	2.0	12.0	2.0	16.0	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_N		20.0	6.0	23.0	6.0	27.0	ns
t_S	Set-up Time HIGH or LOW D_N to LE		4.0	10.0	—	10.0	—	ns
t_H	Hold Time HIGH or LOW D_N to LE		3.0	7.0	—	7.0	—	ns
t_W	LE Pulse Width HIGH or LOW		7.0	10.0	—	10.0	—	ns

HIGH-SPEED CMOS OCTAL D REGISTER (3-STATE)

IDT54/74AHCT374

Integrated Device Technology, Inc.

FEATURES:

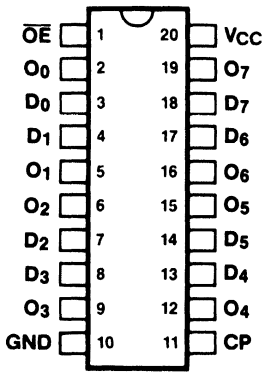
- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical address to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal D register (3-state)
- 100% product assurance screening to MIL-STD-833, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT54/74AHCT374 are 8-bit registers built using advanced CEMOS™II, a dual metal 1.5μm CMOS technology. This register consists of eight D-type flip-flops with a buffered common clock and buffered three-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the three-state conditions.

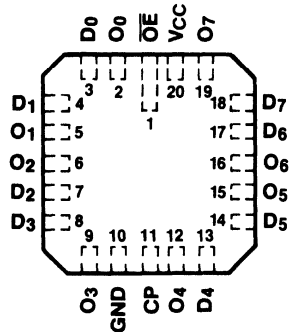
Input data meeting the set-up and hold time requirements of the D inputs is tranferred to the O outputs on the LOW-to-HIGH transition of the clock input.

PIN CONFIGURATIONS



SSDAHCT374-001

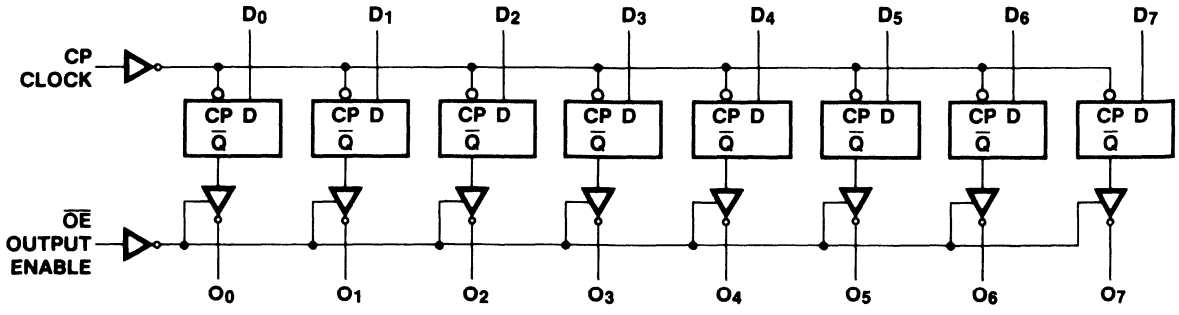
DIP
TOP VIEW



SSDAHCT374-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDAHCT374-003

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL	2.4	4.3	—	
			I_{OH} = -2.6mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-10	µA
			V_O = 2.4V	—	—	10	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 1 MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	2.3	mA
			V_{IN} = 3.4V[4]	—	0.65	4.3	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f/2 \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Clock or latch enable frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_I	The D flip-flop data inputs.
CP	Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.
O_I	The register three-state outputs.
$\overline{OE}$	Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state.

TRUTH TABLE

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	$\overline{OE}$	CLOCK	D_I	O_I	Q_I
Hi-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L	↑	L	L	L
	L	↑	H	H	H
	H	↑	L	Z	L
	H	↑	H	Z	H

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH transition
NC = No Change

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_N	C_L = 50 pf R_L = 500 Ω	10.0	3.0	16.0	3.0	18.0	ns
t_{ZH} t_{ZL}	Output Enable Time		11.0	5.0	18.0	5.0	20.0	ns
t_{HZ} t_{LZ}	Output Disable Time		9.0	2.0	18.0	2.0	24.0	ns
t_S	Setup Time HIGH or LOW D_N to CP		2.0	10.0	—	10.0	—	ns
t_H	Hold Time HIGH or LOW D_N to CP		0.5	3.0	—	4.0	—	ns
t_W	CP Pulse Width HIGH or LOW		10.0	14.0	—	16.5	—	ns

HIGH-SPEED CMOS OCTAL D FLIP-FLOP WITH CLOCK ENABLE

IDT54/74AHCT377

Integrated Device Technology, Inc.

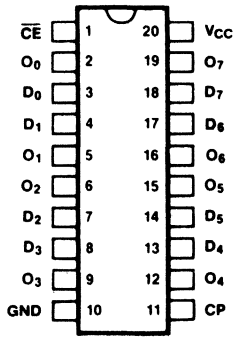
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical clock to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal D flip-flop with clock enable
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

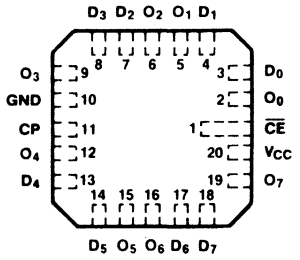
The IDT54/74AHCT377 are octal D flip-flops built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The IDT54/74AHCT377 have eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is LOW. The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

PIN CONFIGURATIONS



SSDFCT377-001

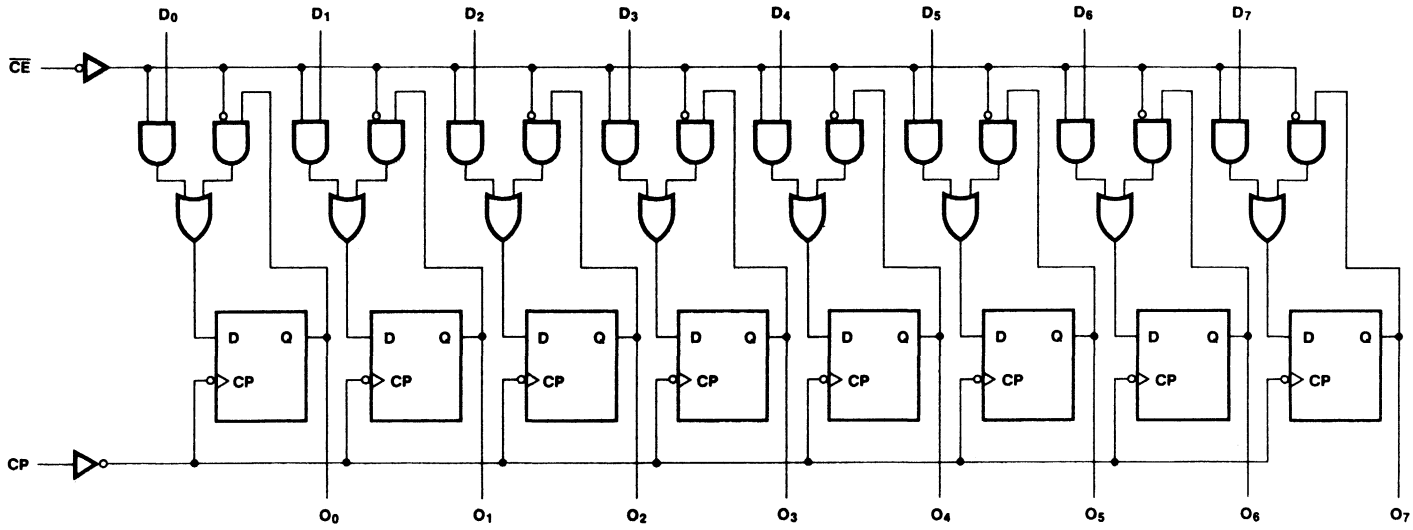
DIP
TOP VIEW



SSDFCT377-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDFCT377-003

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MEMORY INTERFACE

MILITARY AND COMMERCIAL TEMPERATURE RANGES

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL	2.4	4.3	—	
			I_{OH} = -2.6mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 1 MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	0.15	2.3	mA
			V_{IN} = 3.4V[4]	—	0.65	3.3	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f/2 \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Clock or latch enable frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
O_0-O_7	Data Outputs
CP	Clock Pulse Input

TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{CE}$	D_N	O_N
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (Do Nothing)	↑	h	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Immaterial
↑ = LOW-to-HIGH Clock Transition

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_N	C_L = 50pf R_L = 500Ω	10.0	—	—	—	—	ns
t_S	Set Up Time HIGH or LOW D_N to CP		5.0	—	—	—	—	ns
t_H	Hold Time HIGH or LOW D_N to CP		2.0	—	—	—	—	ns
t_S	Set Up Time HIGH or LOW $\overline{CE}$ to CP		5.0	—	—	—	—	ns
t_H	Hold Time HIGH or LOW $\overline{CE}$ to CP		2.0	—	—	—	—	ns
t_W	Clock Pulse Width, LOW		7.0	—	—	—	—	ns

HIGH-SPEED CMOS 8-BIT IDENTITY COMPARATOR

IDT54/74AHCT521

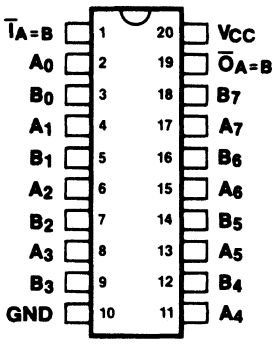
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 9ns typical propagation delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- 8-bit identity comparator
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT54/74AHCT521 are 8-bit identity comparators built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The device compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

PIN CONFIGURATIONS



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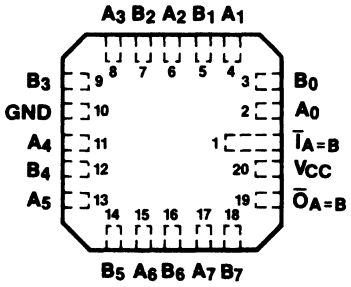
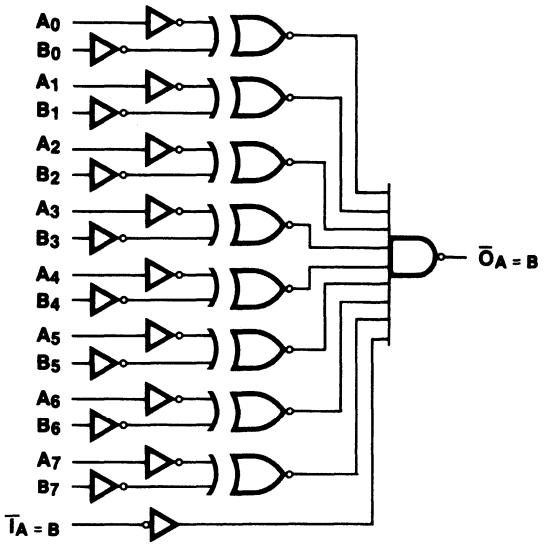
DIP
TOP VIEW



SSDAHCT521-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -200µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	—	mA/ MHz
I_{CC}	Total Power Supply Current	V_{CC} = Max. f = 1 MHz Outputs Open One Input Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	—	mA
			V_{IN} = 3.4V[4]	—	0.65	—	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
A_0-A_7	Word A inputs
B_0-B_7	Word B inputs
$\overline{I}_{A=B}$	Expansion or Enable Input (Active LOW)
$\overline{O}_{A=B}$	Identity Output (Active Low)

TRUTH TABLE

INPUTS		OUTPUT
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A_N or B_N to $\overline{O}_{A=B}$	C_L = 50 pf R_L = 500 Ω	9.0	—	—	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$		5.0	—	—	—	—	ns

HIGH-SPEED CMOS OCTAL TRANSPARENT LATCH (3-STATE)

IDT54/74AHCT533

Integrated Device Technology, Inc.

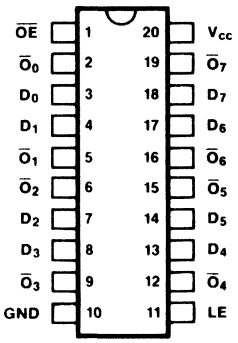
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 11ns typical clock to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μ max.)
- Octal transparent latch with 3-state output
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

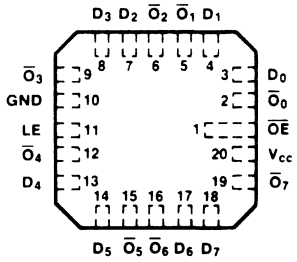
The IDT54/74AHCT533 are octal transparent latches built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The IDT54/74AHCT533 consist of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

PIN CONFIGURATIONS



SSDFCT533-001

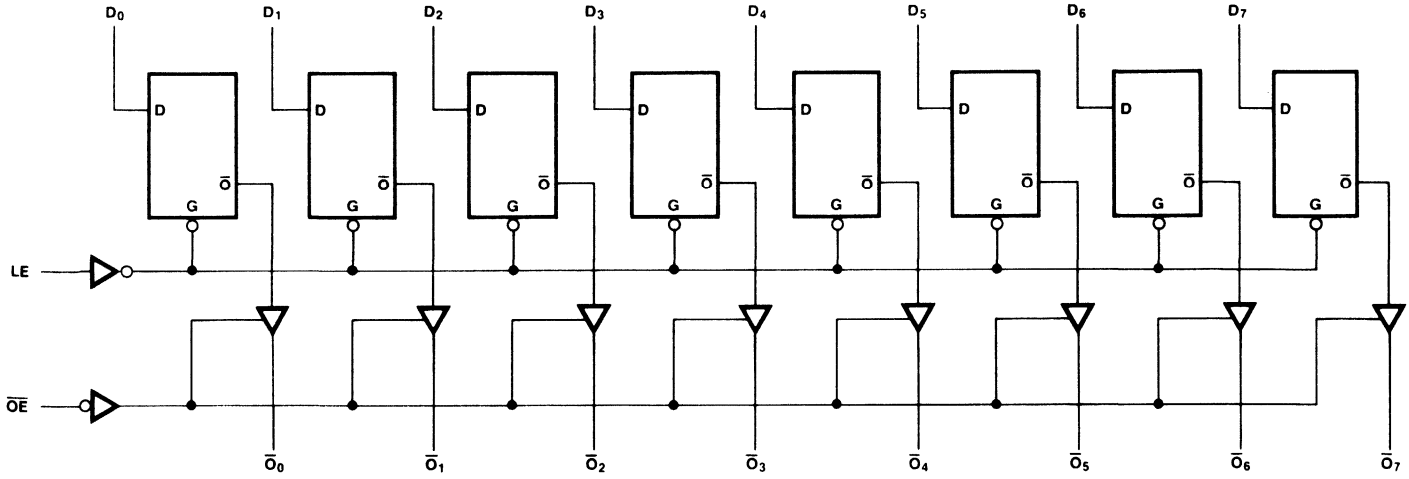
DIP
TOP VIEW



SSDFCT533-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDAHCT533-003

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MEMORY INTERFACE

MILITARY AND COMMERCIAL TEMPERATURE RANGES

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL	2.4	4.3	—	
			I_{OH} = -2.6mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-10	µA
			V_O = 2.4V	—	—	10	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN} \le V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 1 MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	0.15	2.3	mA
			V_{IN} = 3.4V[4]	—	0.65	4.3	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f/2 \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Clock or latch enable frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{O}_0$-$\overline{O}_7$	Complementary 3-State Outputs

TRUTH TABLE

INPUTS		OUTPUTS	
D_N	LE	$\overline{OE}$	$\overline{O}_N$
H	H	L	L
L	H	L	H
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_N to $\overline{O}_N$	C_L = 50pf R_L = 500Ω	11.0	4.0	19.0	4.0	24.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	4.0	18.0	4.0	20.0	ns
t_{HZ} t_{LZ}	Output Disable Time		11.0	2.0	16.0	2.0	22.0	ns
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_N$		15.0	4.0	23.0	4.0	28.0	ns
t_S	Set Up Time HIGH or LOW D_N to LE		7.0	15.0	—	15.0	—	ns
t_H	Hold Time HIGH or LOW D_N to LE		5.0	7.0	—	7.0	—	ns
t_W	LE Pulse Width HIGH or LOW		7.0	15.0	—	15.0	—	ns

Integrated Device Technology Inc

HIGH-SPEED CMOS OCTAL D FLIP-FLOP (3-STATE)

IDT54/74AHCT534

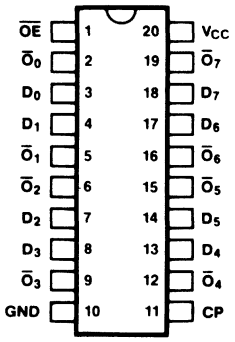
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical clock to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal D flip-flop with 3-state output
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

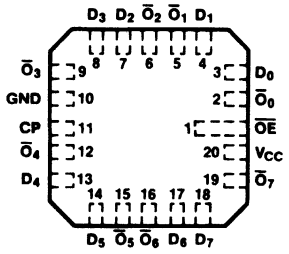
The IDT54/74AHCT534 are octal D flip-flops built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The IDT54/74FCT534 are high-speed, low-power octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

PIN CONFIGURATIONS



SSDFCT534-001

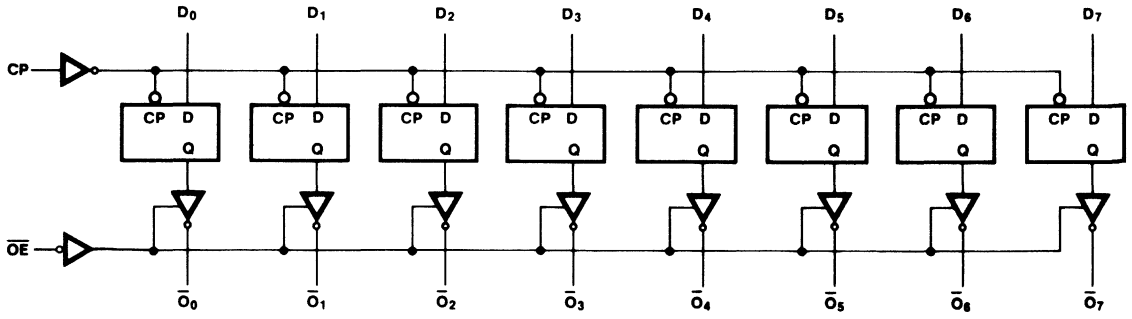
DIP
TOP VIEW



SSDFCT534-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL	2.4	4.3	—	
			I_{OH} = -2.6mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-10	µA
			V_O = 2.4V	—	—	10	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 1 MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	2.3	mA
			V_{IN} = 3.4V[4]	—	0.65	4.3	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f/2 \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Clock or latch enable frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	3-State Output Enable Input (Active LOW)
$\overline{O}_0$-$\overline{O}_7$	Complementary 3-State Outputs

TRUTH TABLE

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	$\overline{OE}$	CP	D_I	$\overline{O}_N$	Q_I
Hi-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L	↑	L	H	H
	L	↑	H	L	L
	H	↑	L	Z	H
	H	↑	H	Z	L

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH transition
NC = No Change

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_N$	C_L = 50 pf R_L = 500Ω	10.0	3.0	16.0	3.0	18.0	ns
t_{ZH} t_{ZL}	Output Enable Time		11.0	5.0	18.0	5.0	20.0	ns
t_{HZ} t_{LZ}	Output Disable Time		11.0	2.0	14.0	2.0	16.0	ns
t_S	Set Up Time HIGH or LOW D_N to CP		2.0	10.0	—	10.0	—	ns
t_H	Hold Time HIGH or LOW D_N to CP		0.5	3.0	—	4.0	—	ns
t_W	CP Pulse Width HIGH or LOW		7.0	14.0	—	16.0	—	ns

HIGH-SPEED CMOS OCTAL INVERTING BUFFER TRANSCEIVER

IDT54/74AHCT640

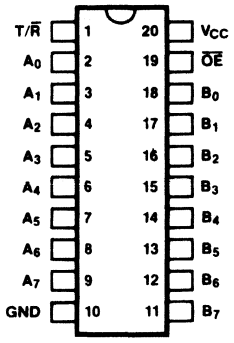
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns data to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Inverting buffer transceiver
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

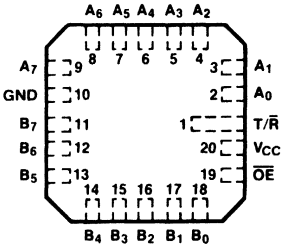
The IDT54/74AHCT640 are 8-bit inverting buffer transceivers built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (T/$\overline{R}$) input. The enable input ($\overline{OE}$) can be used to disable the device so the buses are effectively isolated.

PIN CONFIGURATIONS



SSDAHCT640-001

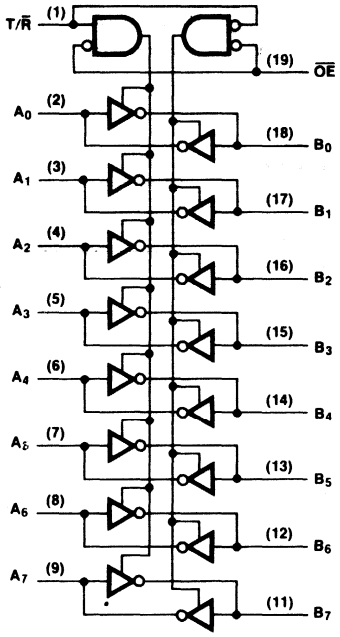
DIP
TOP VIEW



SSDAHCT640-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDAHCT640-003

MEMORY INTERFACE

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-15	µA
			V_O = 2.4V	—	—	15	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN} \le V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 10 MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \le V_{IN} \le V_{LC}$	—	1.5	4.5	mA
			V_{IN} = 3.4V[4]	—	2.0	5.5	
$V_+ - V_-$	Hysteresis	$\overline{OE}$ and all D Inputs		—	0.2	—	V

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V).
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V).

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_7	Side B Inputs or 3-State Outputs

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A	C_L = 50 pf R_L = 500 Ω	10.0	2.0	11.0	2.0	14.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	5.0	24.0	5.0	27.0	ns
t_{HZ} t_{LZ}	Output Disable Time		12.0	2.0	15.0	2.0	20.0	ns

Integrated Device Technology, Inc.

HIGH-SPEED CMOS NON-INVERTING BUFFER TRANSCEIVER

IDT54/74AHCT645

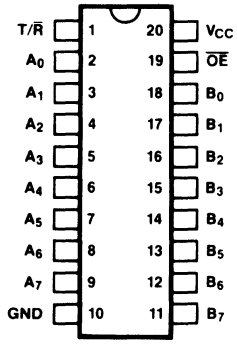
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 8ns typical data to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Non-inverting buffer transceiver
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT54/74AHCT645 are 8-bit non-inverting buffer transceivers built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. These non-inverting buffer transceivers are designed for ansynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control (T/$\overline{R}$) input. The enable input ($\overline{OE}$) can be used to disable the device so the buses are effectively isolated.

PIN CONFIGURATIONS



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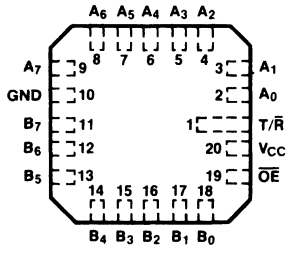

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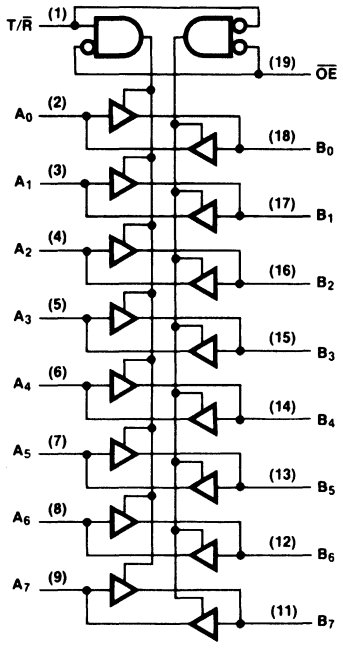
LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Cont'd)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-15	µA
			V_O = 2.4V	—	—	15	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4 V[4]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[5] Current	V_{CC} = Max. f = 1 MHz Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	2.3	mA
			V_{IN} = 3.4V[4]	—	0.65	3.3	
$V_+ - V_-$	Hysteresis	$\overline{OE}$ and all Data Inputs		—	0.2	—	V

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3 4V).
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V).

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_7	Side B Inputs or 3-State Outputs

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

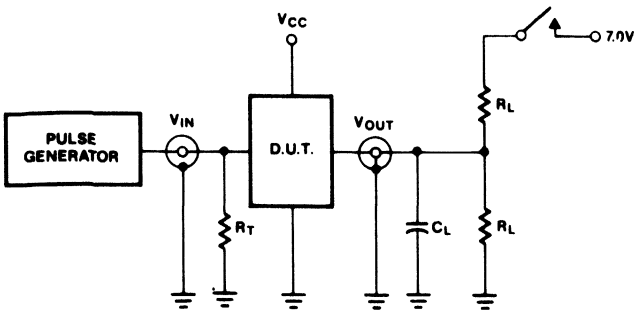
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B B to A	C_L = 50 pf R_L = 500Ω	8.0	3.0	10.0	3.0	15.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	5.0	20.0	5.0	25.0	ns
t_{HZ} t_{LZ}	Output Disable Time		11.0	2.0	15.0	2.0	18.0	ns
t_{DLH} t_{DHL}	Propagation Delay T/$\overline{R}$ to A or B*		15.0	—	—	—	—	ns

*Guaranteed by Design

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR THREE-STATE OUTPUTS



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SWITCH POSITION

TEST	SWITCH
t_{LZ}	Closed
t_{ZL}	Closed
All Other	Open

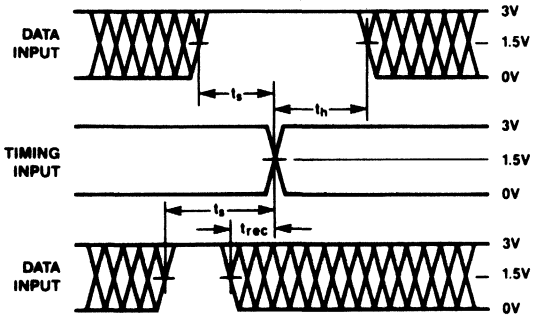
DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination should be equal to Z_{OUT} of pulse generators.

SET-UP, HOLD, AND RELEASE TIMES



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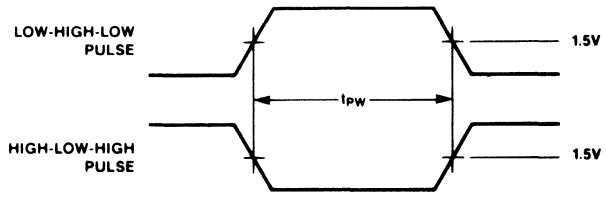
PULSE WIDTH



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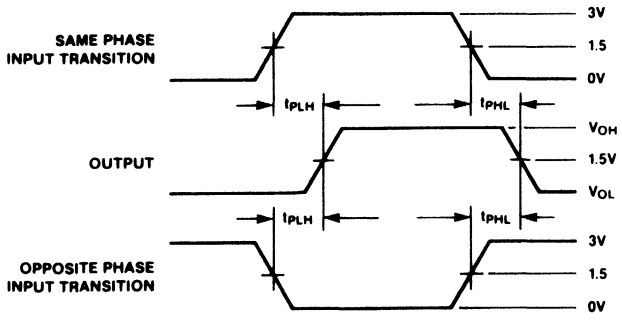
PROPAGATION DELAY



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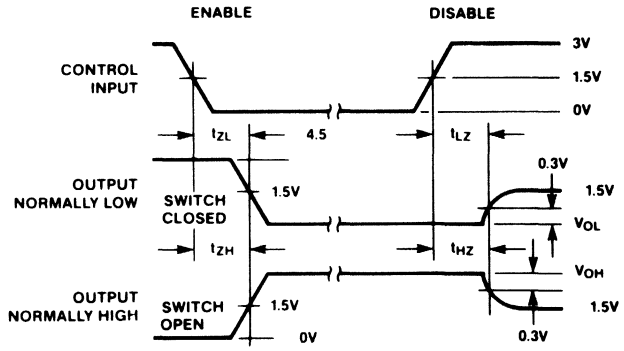
ENABLE AND DISABLE TIMES



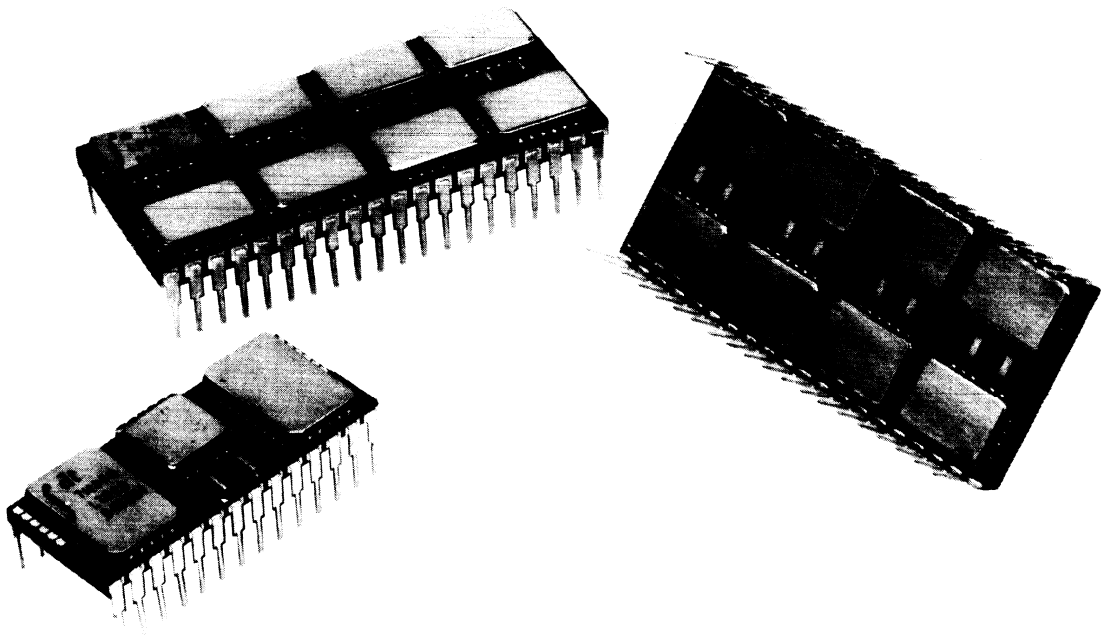
SSDAHCT645-008

NOTES:

1. Diagram shown for input Control Enable-LOW and Input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_O = 50Ω; t_r ≤ 2.5ns; t_f ≤ 2.5ns.

HIGH-SPEED CMOS SUBSYSTEMS PRODUCTS

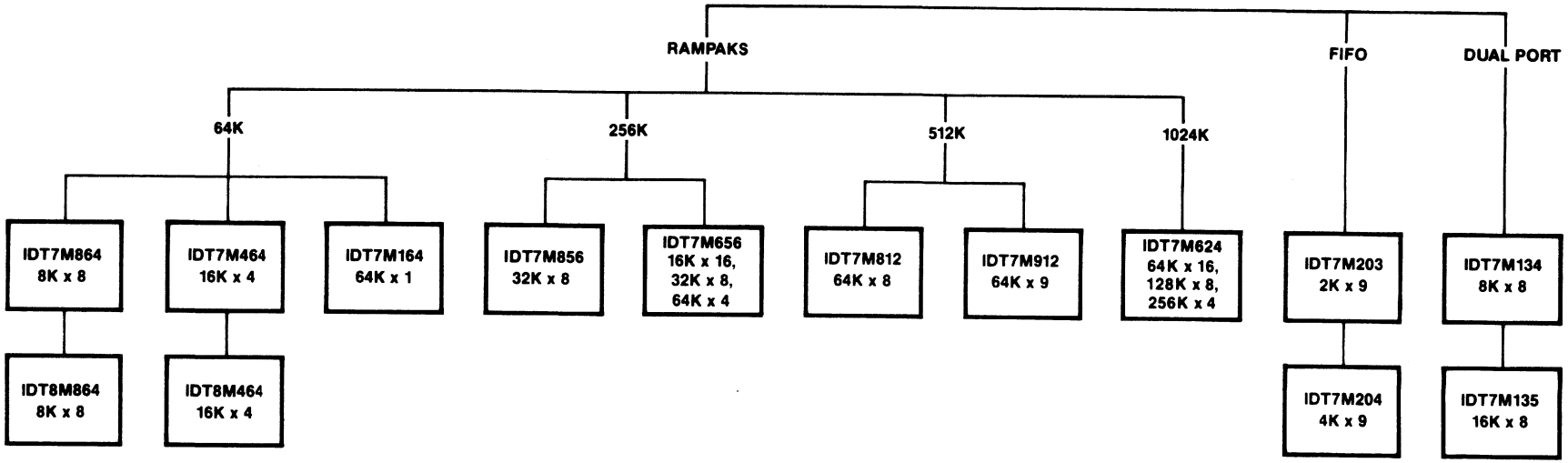
CONTENTS **PAGE**



Integrated Device Technology, Inc.

LEADING THE CMOS FUTURE

SUBSYSTEM MODULES



Integrated Device Technology Inc

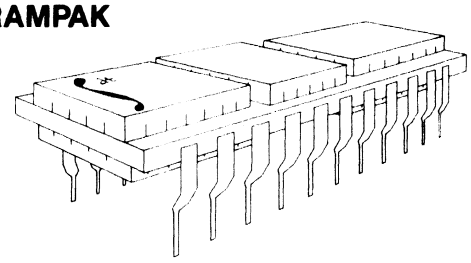
64K (64K x 1) CMOS STATIC RAMPAK

IDT7M164

FEATURES:

- 65,536x1 bit static RAM module complete with decoder and decoupling capacitor
- High-speed 60 (commercial only)/70/85/100ns (equal access and cycle times)
- Low power consumption, 250mW typically
- Offered in a 22 pin, 300 mil center sidebrase DIP
- Pin compatible with proposed monolithics
- Utilizes IDT6167s — high performance 16K RAMs produced with advanced CEMOS™I technology
- CEMOS I process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (+10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clock or refresh required
- Military modules available with semiconductor components 100% screened to MIL-STD-883 Class B

64K RAMPAK



DESCRIPTION:

The IDT7M164 is a 64K (65,536x1 bit) high speed static RAM constructed on a ceramic substrate using 4 IDT6167 (16Kx1) static RAMs in leadless chip carriers. Functional equivalence to proposed monolithic 64Kx1 static RAM is achieved by utilization of an on-board decoder circuit that interprets the higher order addresses A_{14} and A_{15} to select one of the four 16Kx1 RAMs. Extremely fast speeds can be achieved with this technique due to use of the IDT6167, fabricated in IDT's high performance, high-reliability technology — CEMOS™I. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 16K static RAMs available.

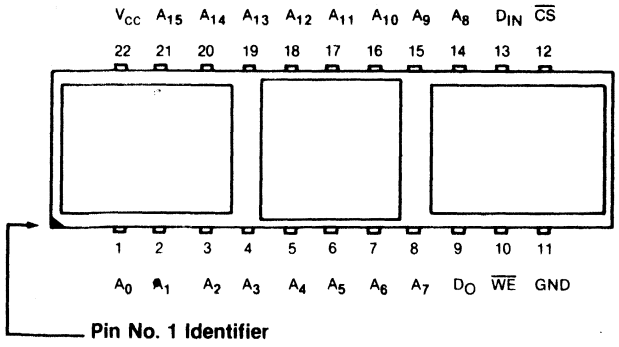
The IDT7M164 is available with access times as fast as 60ns for commercial and 70ns for military temperature ranges, with maximum power consumption of only 605mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as this condition is held. In the standby mode, the module typically consumes less than 100 mW. Substantially lower power levels can be achieved in the ISB_1 mode (less than 50 μW typ.) and 2V data retention mode (less than 4 μW typ.) - see "DC Characteristics" and "Data Retention Characteristics" for details.

The IDT7M164 is offered in a space saving 22-pin, 300 mil pin center package, providing equivalent pinout to the proposed monolithic 64Kx1 static RAMs.

All inputs and outputs of the IDT7M164 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Full asyncronous circuitry is used, requiring no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

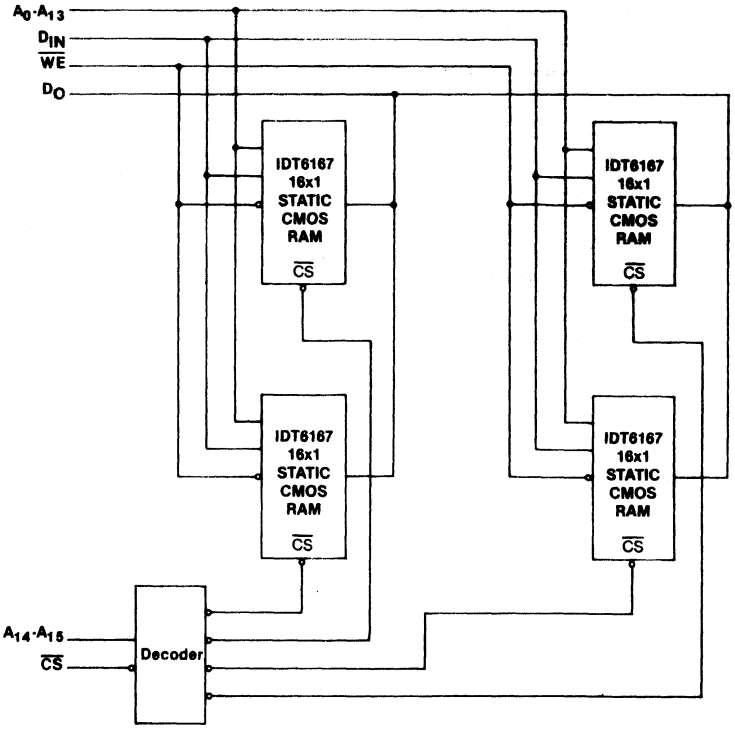
All IDT module semiconductor components are processed in compliance to the test methods of MIL-STD-883, as shown on back of data sheet, making them ideally suited for applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



IDT7M164
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0-A_{15}	ADDRESS	$\overline{WE}$	WRITE ENABLE
D_{IN}	DATA INPUT	D_O	DATA OUTPUT
$\overline{CS}$	CHIP SELECT	GND	GROUND
V_{CC}	POWER		

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SUBSYSTEMS

MILITARY AND COMMERCIAL TEMPERATURE RANGES

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TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

RECOMMENDED DC OPERATING CONDITIONS

(T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−0.5 *	—	+0.8	V

*V_{IL} min = −1.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M164 MIN.	TYP.(1)	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open	—	50	110	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	50	110	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$	—	20	80	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{CC}$ − 0.2V $V_{IN} \geq V_{CC}$ − 0.2V or $\leq$ 0.2V	—	0.008	3.6(2)	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4mA	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C
2. I_{SB1}max at commercial temperature = 1.0 mA

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−10 to +85	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	4.0	4.0	W
I_{OUT}	DC Output Current	50	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

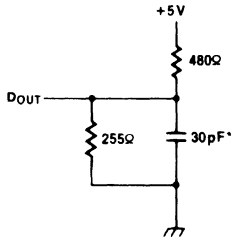


Figure 1. Output Load

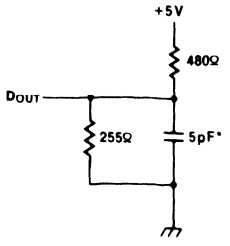


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

*Including scope and jig.

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

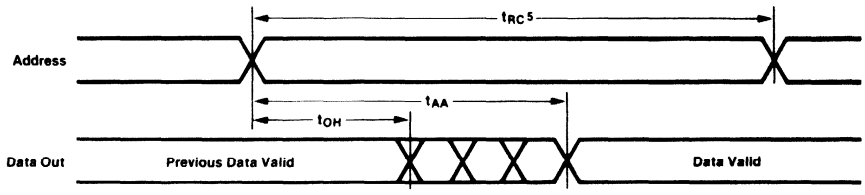
SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE: This parameter is sampled and not 100% tested.

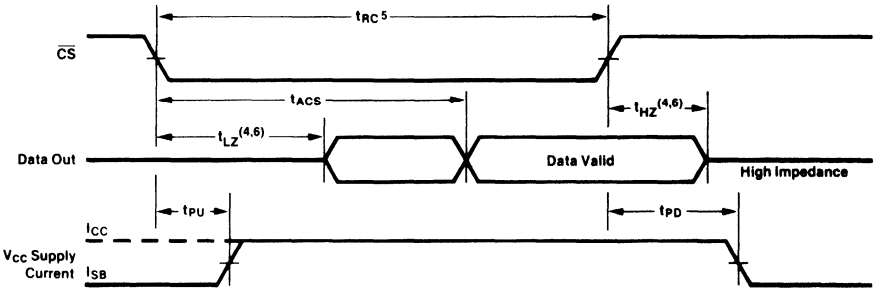
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	IDT7M164L60 COMMERCIAL ONLY		IDT7M164L70		IDT7M164L85		IDT7M164L100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE										
t_{RC}	Read Cycle Time	60	—	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	60	—	70	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	60	—	70	—	85	—	100	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	10	—	ns
t_{LZ}	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{HZ}	Chip Deselection to Output in High Z	0	50	0	55	0	60	0	70	ns
t_{PU}	Chip Selection to Power Up Time	15	—	15	—	20	—	30	—	ns
t_{PD}	Chip Deselection to Power Down Time	—	60	—	70	—	85	—	100	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	60	—	70	—	85	—	100	—	ns
t_{CW}	Chip Selection to End of Write	55	—	65	—	75	—	80	—	ns
t_{AW}	Address Valid to End of Write	55	—	65	—	75	—	80	—	ns
t_{AS}	Address Setup Time	15	—	20	—	20	—	25	—	ns
t_{WP}	Write Pulse Width	35	—	40	—	45	—	45	—	ns
t_{WRW}	Write Recovery Time WE Controlled	0	—	0	—	0	—	0	—	ns
t_{WRC}	Write Recovery Time CS Controlled	15	—	25	—	25	—	25	—	ns
t_{DW}	Data Valid to End of Write	25	—	25	—	30	—	30	—	ns
t_{DHW}	Data Hold Time WE Controlled	0	—	0	—	0	—	0	—	ns
t_{DHC}	Data Hold Time CS Controlled	15	—	25	—	25	—	25	—	ns
t_{WZ}	Write Enable to Output in High Z	0	30	0	40	0	40	0	40	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

TIMING WAVEFORM OF READ CYCLE NO. 1[1,2]



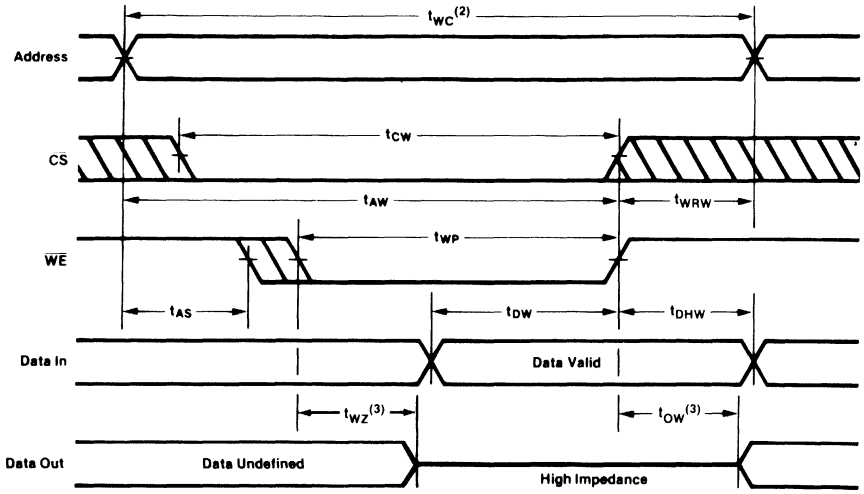
TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]



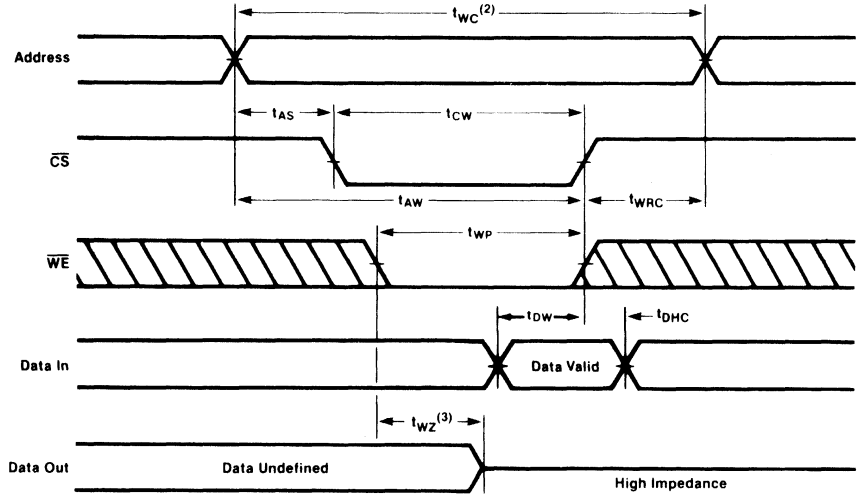
NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. For any given speed grade, operating voltage, and temperature, t_{HZ} will be less than or equal to t_{LZ}.

SUBSYSTEMS

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1)



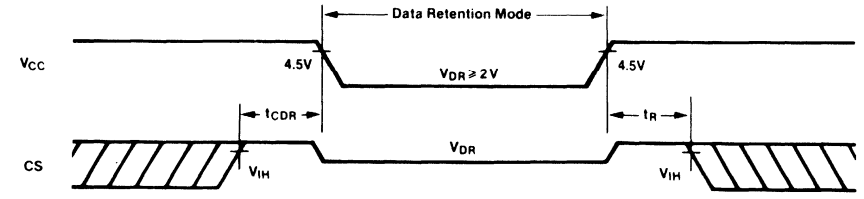
NOTES: 1. $\overline{WE}$ or $\overline{CS}$ must be high during address transitions.
2. All write cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ± 100mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.(1)	MAX. COMM.	MAX. MIL.	UNIT
V_{DR}	V_{CC} for Data Retention		2.0	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ −0.2V	—	2.0(2)	300(2)	1200	µA
			—	4.0(3)	450(3)	1800	
t_{CDR}	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC}$ −0.2V or ≤ 0.2V	0	—	—	—	ns
t_R	Operation Recovery Time		t_{RC}(4)	—	—	—	ns

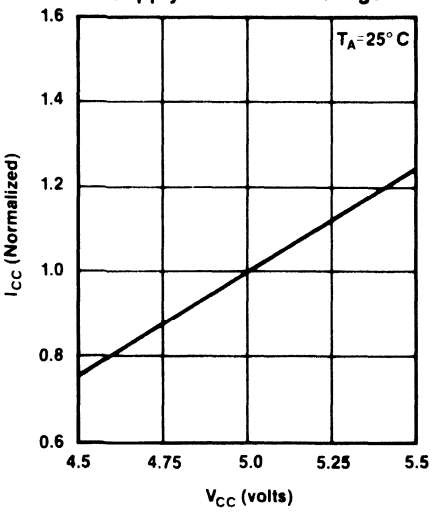
NOTES: 1. T_A = 25°C
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM

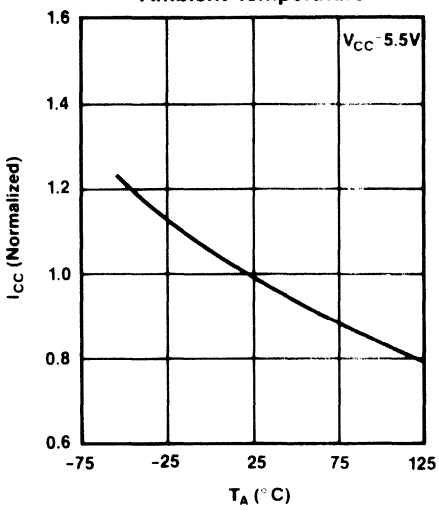


NORMALIZED TYPICAL PERFORMANCE CHARACTERISTICS

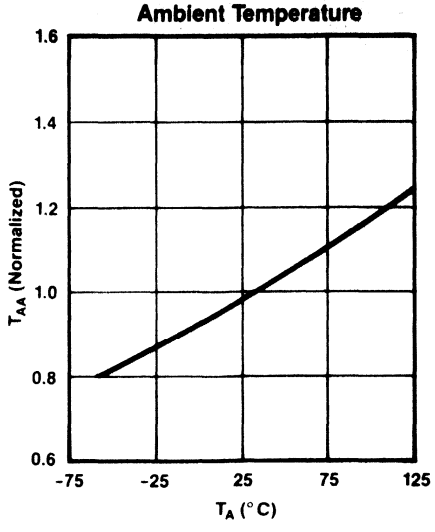
Supply Current vs. Voltage



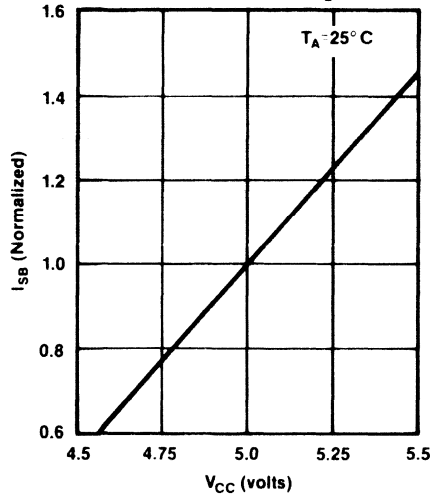
Supply Current vs. Ambient Temperature



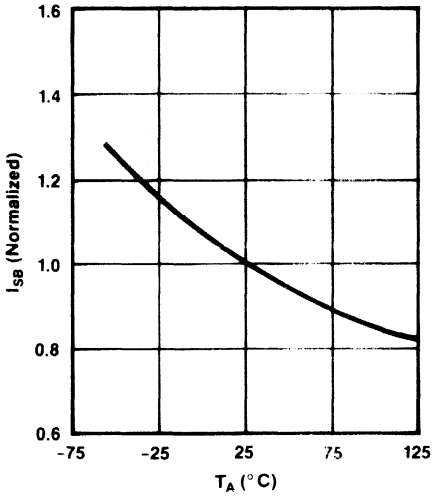
Address Access Time vs. Ambient Temperature



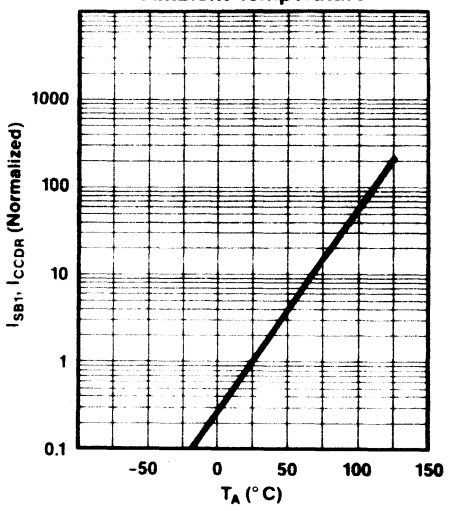
Stand-by Power Supply Current vs. Voltage



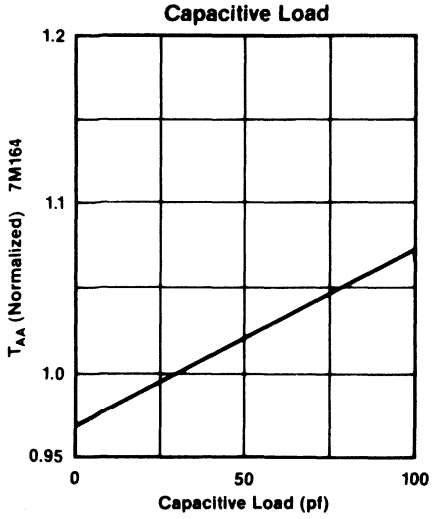
Stand-by Power Supply Current vs. Ambient Temperature



Full Stand-by Power Supply Current. Data Retention Current vs. Ambient Temperature



Address Access Time vs. Capacitive Load



SUBSYSTEMS

Integrated Device Technology, Inc.

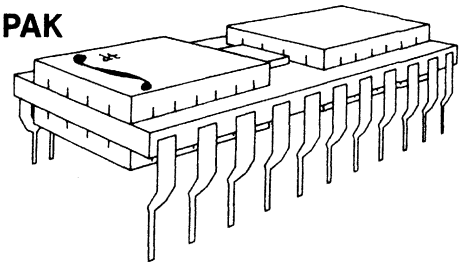
64K (16K x 4) CMOS STATIC RAMPAK

IDT7M464 IDT8M464

FEATURES:

- IDT7M464 equivalent to JEDEC standard 16Kx4 monolithic RAM
- 65,536 bit CMOS statis RAM module with decoupling capacitor
- High-speed: 55/65/85ns max. commercial
  65/85/100ns max. military
- Low power consumption: 1.1W max.
- IDT7M464 pinout identical to proposed monolithic 16Kx4 static RAMs
- IDT8M464 package options reduces overall height
- Utilizes IDT6167s — high performance 16K RAMs produced with advanced CEMOS™I technology
- CEMOS I process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Military modules available with semiconductor components 100% screened to Mil-STD-883 class B.

64K RAMPAK



DESCRIPTION:

The IDT7M464/IDT8M464 are 64K (16,384 x 4 bit) high speed CMOS static RAMs constructed on ceramic substrates using 4 IDT6167 (16,384 x 1 bit) CMOS static RAMs in leadless chip carriers. Functional equivalence to proposed monolithic 16Kx4 static RAMs is achieved by utilization of tungsten traces with the substrate to connect the four 16K RAMs in a 16Kx4 configuration. Extremely fast speeds can be achieved with this technique due to use of the IDT6167, fabricated in IDT's high-performance, high-reliability technology — CEMOS™I. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 16K static RAMs available.

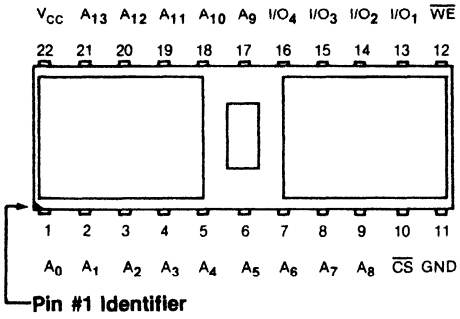
The IDT7M464/IDT8M464 are available with access times as fast as 55ns for commercial and 65ns for military temperature ranges, with maximum power consumption of only 1.1 watt. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high, consuming only 440mW maximum. Substantially lower power levels can be achieved in the I_{SB1} mode (less than 20mW max.) and 2V data retention mode (less than 3mW max.) - see "DC Characteristics" and "Data Retention Characteristics" for details.

The IDT7M464 is offered in a space saving 22-pin, 300 mil pin center package, providing equivalent pinout to the proposed monolithic 16Kx4 static RAMs. The IDT8M464 is offered in a 22-pin, 400 mil pin center package reducing overall package height.

All inputs and outputs of the IDT7M464/IDT8M464 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Full asyncronous circuitry is used, requiring no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

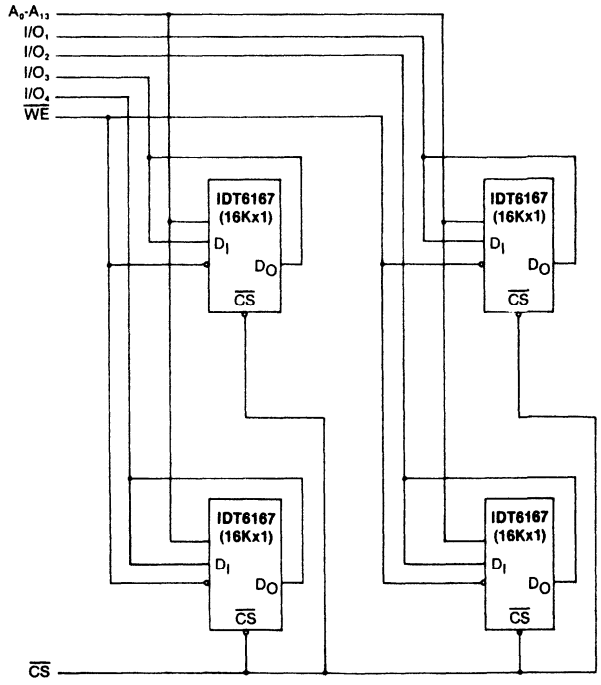
All IDT module semiconductor components are processed in compliance to the test methods of MIL-STD-883, as shown on back of data sheet, making them ideally suited for applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



IDT7M464/IDT8M464
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0–A_{13}	ADDRESS	$\overline{WE}$	WRITE ENABLE
I/O_1–I/O_4	DATA INPUT/OUTPUT	V_{CC}	POWER
$\overline{CS}$	CHIP SELECT	GND	GROUND

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TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

RECOMMENDED DC OPERATING CONDITIONS

(T_A = −55°C to +125°C and 0°C to + 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	−0.5*	—	0.8	V

*V_{IL} min = 1.0V for pulse width loss than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M464 MIN.	IDT7M464 TYP.(1)	IDT7M464 MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open	—	100	200	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	100	200	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$	—	20	80	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{CC}$ − 0.2V $V_{IN} \geq V_{CC}$ − 0.2V or $\leq$ 0.2V	—	.008	3.6(2)	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4mA	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C
2. I_{SB1} max at commercial temperature = 1.0 mA

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−10 to +85	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	4.0	4.0	W
I_{OUT}	DC Output Current	50	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

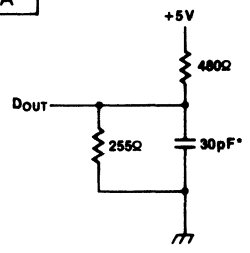


Figure 1. Output Load

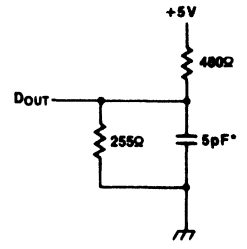


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

*Including scope and jig.

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	30	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	22	pF

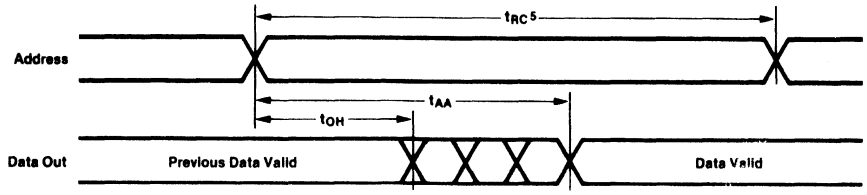
NOTE: This parameter is sampled and not 100% tested.

SUBSYSTEMS

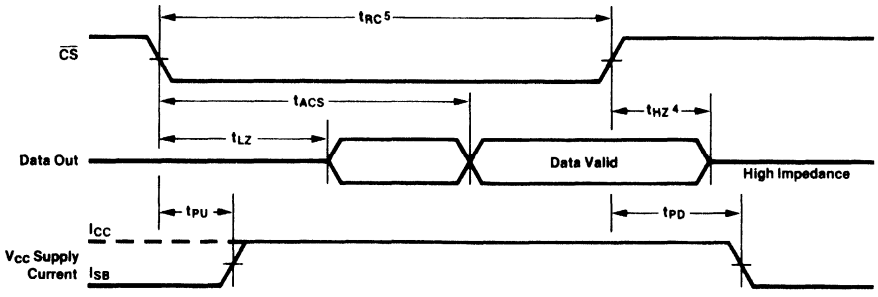
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	7M464S55 COMMERCIAL ONLY MIN.	MAX.	7M464S65 MIN.	MAX.	7M464S85 MIN.	MAX.	7M464S100 MILITARY ONLY MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	55	—	65	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	65	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	55	—	65	—	85	—	100	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{LZ}	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{HZ}	Chip Deselection to Output in High Z	0	40	0	40	0	50	0	50	ns
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselection to Power Down Time	—	55	—	65	—	85	—	100	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	55	—	65	—	85	—	100	—	ns
t_{CW}	Chip Selection to End of Write	45	—	55	—	65	—	80	—	ns
t_{AW}	Address Valid to End of Write	45	—	55	—	65	—	80	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	35	—	40	—	45	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	25	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High Z	0	40	0	40	0	50	0	50	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

TIMING WAVEFORM OF READ CYCLE NO. 1[1,2]

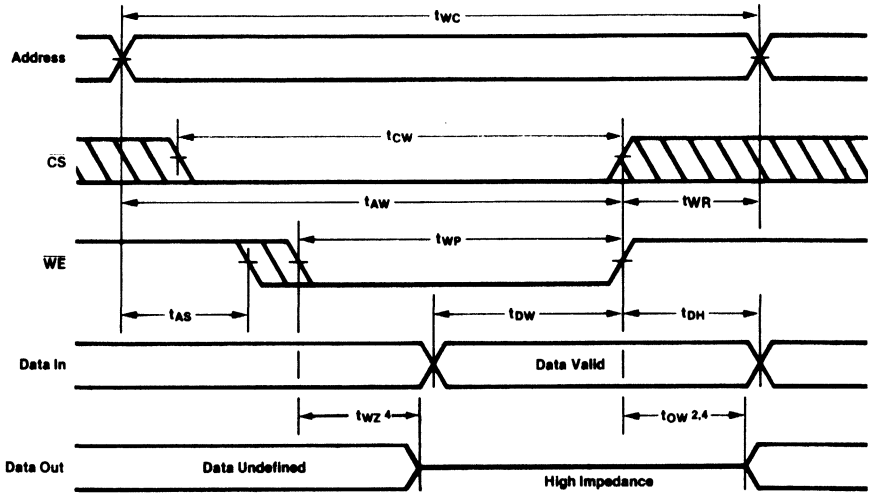


TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]

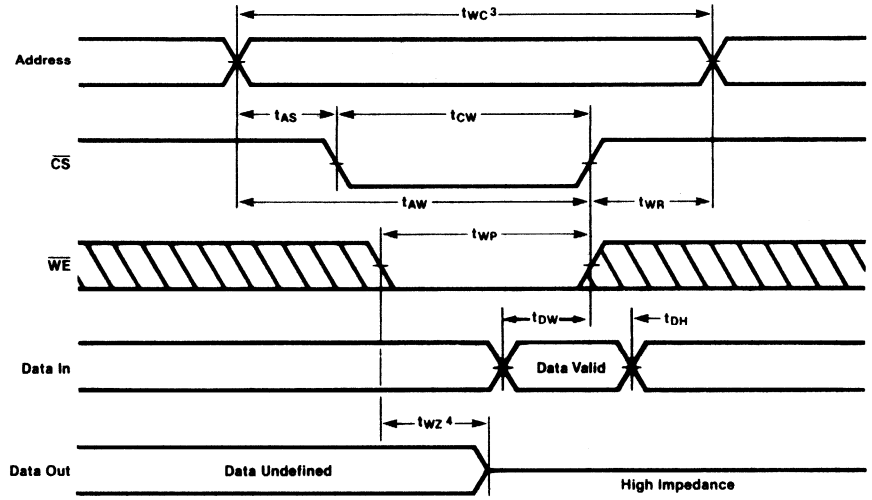


NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. For any given speed grade, operating voltage, and temperature, t_{HZ} will be less than or equal to t_{LZ}.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1]



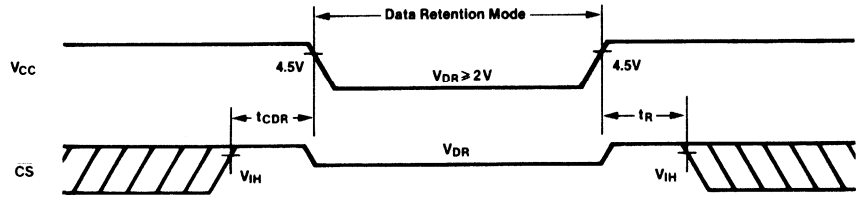
NOTES: 1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.(1)	MAX COMM.	MAX. MIL.	UNIT
V_{DR}	V_{CC} for Data Retention		2.0	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ −0.2V	— —	2.0(2) 4.0(3)	250(2) 375(3)	1200 1800	µA
t_{CDR}	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC}$ −0.2V or ≤ 0.2V	0	—	—	—	ns
t_R	Operation Recovery Time		t_{RC}(4)	—	—	—	ns

NOTES: 1. T_A = 25°C
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time

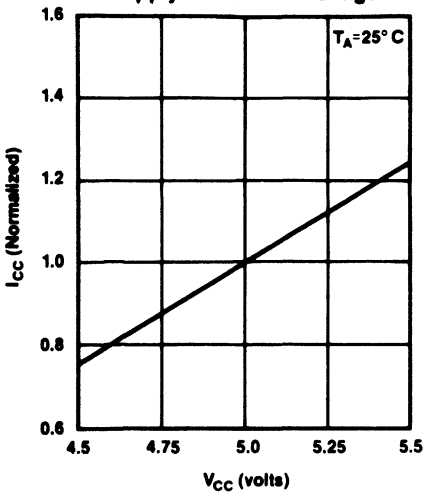
LOW V_{CC} DATA RETENTION WAVEFORM



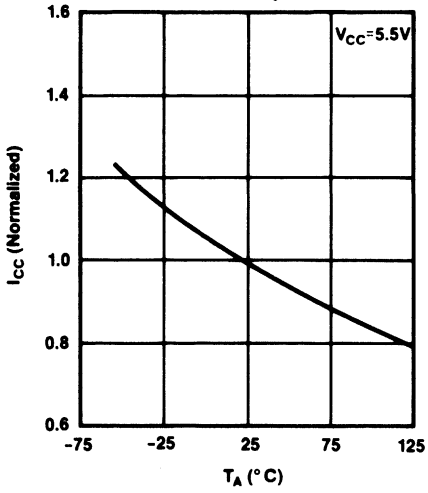
SUBSYSTEMS

NORMALIZED TYPICAL PERFORMANCE CHARACTERISTICS

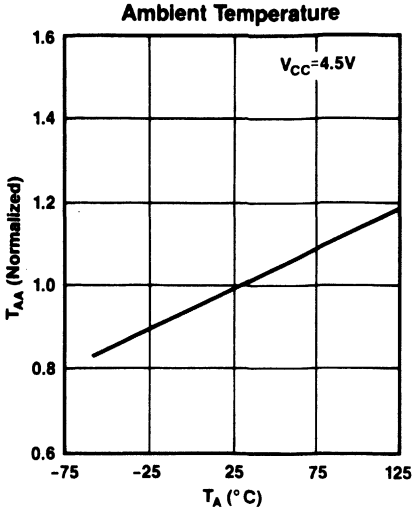
Supply Current vs. Voltage



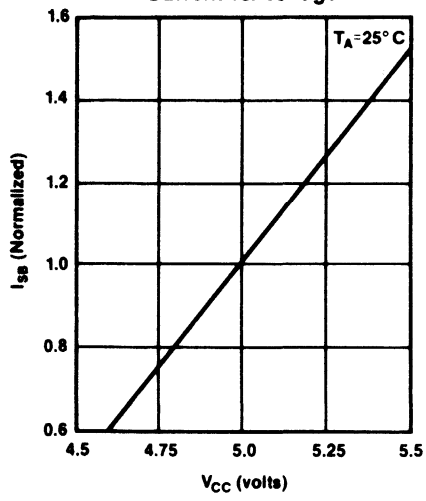
Supply Current vs. Ambient Temperature



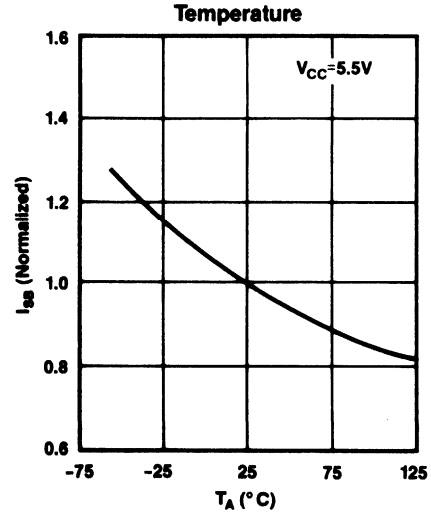
Address Access Time vs. Ambient Temperature



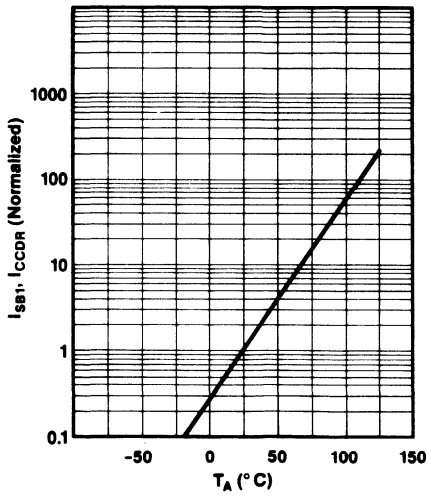
Stand-by Power Supply Current vs. Voltage



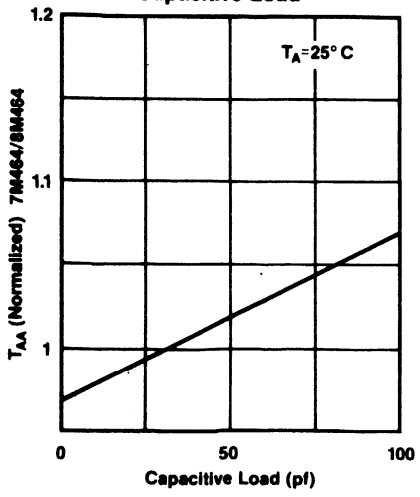
Stand-by-Power Supply Current vs. Ambient Temperature



Full Stand-by Power Supply Current. Data Retention Current vs. Ambient Temperature



Address Access Time vs. Capacitive Load



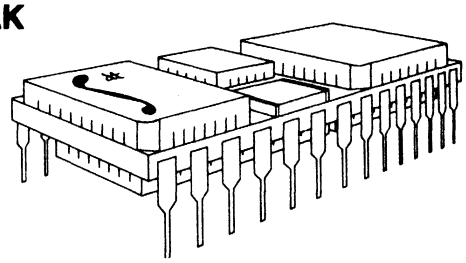
64K (8K x 8) CMOS STATIC RAMPAK

IDT7M864
IDT8M864

FEATURES:

- Equivalent to JEDEC standard 8K x 8 monolithic RAM
- 8,192 x 8 CMOS static RAM module complete with decoder and decoupling capacitor
- High-speed 65 (commercial only) 75/85/120/150/200ns (equal access and cycle times)
- Low power consumption, less than 1 watt maximum
- Two pinout options (64K EPROM & 64K static RAM)
- Utilizes IDT6116s — high performance 16K RAMs produced with advanced CEMOS™I technology
- CEMOS I process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Military modules available with semiconductor components 100% screened to MIL-STD-883 Class B

64K RAMPAK



The IDT7M864/IDT8M864 are available with access times as fast as 65ns for commercial and 75ns for military temperature ranges, with maximum power consumption of only 990mW. The circuit also offers a reduced power standby mode. When $\overline{CS}_1$ high and/or CS_2 (7M864) goes low, the circuit will automatically go to, and remain in, a standby mode as long as these conditions are held. In the standby mode, the module consumes less than 440mW. Substantially lower power levels can be achieved in the I_{SB1} mode (less than 20mW max.) and 2V data retention mode (less than 3mW max.) - see "DC Characteristics" and "Data Retention Characteristics" for details.

Pinout of the IDT8M864 is equivalent to the 64K EPROMs (no connect on pin 26), ideal for applications requiring easy microcode changes during prototyping. The IDT7M864's pinout is compatible with monolithic 64K static RAMs (CS_2 on pin 26).

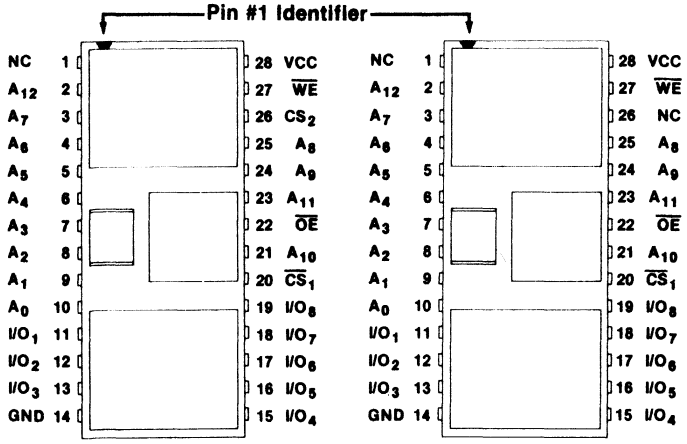
All inputs and outputs of the IDT7M864/IDT8M864 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Full asyncronous circuitry is used, requiring no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

All IDT module semiconductor components are processed in compliance to the test methods of MIL-STD-883, as shown on back of data sheet, making them ideally, suited for applications demanding the highest level of performance and reliability.

DESCRIPTION:

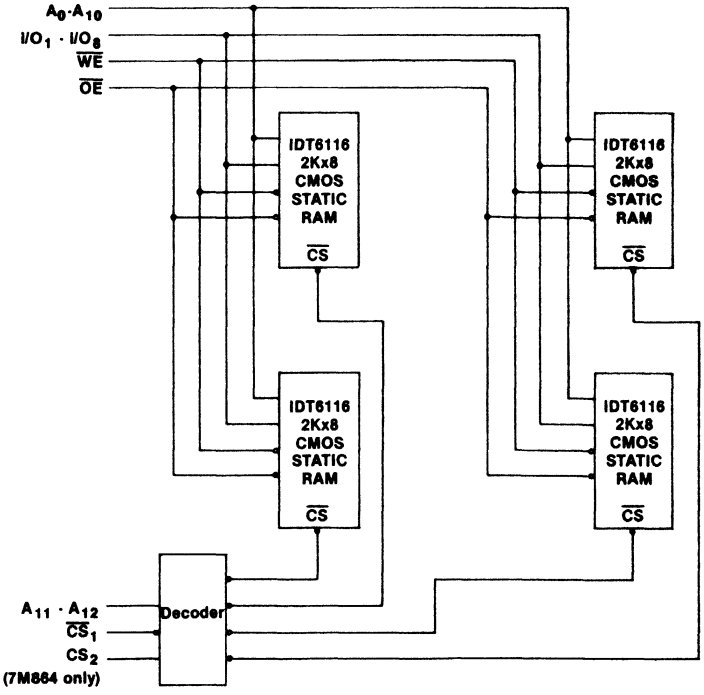
The IDT7M864/IDT8M864 are 64K (8,192 x 8 bit) high speed static RAMs constructed on a ceramic substrate using 4 IDT6116 (2,048 x 8) static RAMs in leadless chip carriers. Functional equivalence to a monolithic 64K static RAM is achieved by utilization of an on-board decoder circuit that interprets the higher order addresses A_{11} and A_{12} to select one of the four 2Kx8 RAMs. Extremely fast speeds can be achieved with this technique due to use of the IDT6116 fabricated in IDT's high performance, high-reliability technology — CEMOS™I. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 16K static RAMs available.

PIN CONFIGURATIONS



7M864 **8M864**

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0-A_{12}	ADDRESS	$\overline{WE}$	WRITE ENABLE
I/O_1-I/O_8	DATA INPUT/OUTPUT	$\overline{OE}$	OUTPUT ENABLE
$\overline{CS}_1$, CS_2	CHIP SELECT	GND	GROUND
V_{CC}	POWER		

CEMOS is a trademark of Integrated Device Technology, Inc.

SUBSYSTEMS

MILITARY AND COMMERCIAL TEMPERATURE RANGES

TRUTH TABLE

MODE	$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	I/O OPERATION
Standby	H	X	X	X	High Z
Standby	X	L	X	X	High Z
Read	L	H	L	H	D_{OUT}
Read	L	H	H	H	High Z
Write	L	H	X	L	D_{IN}

RECOMMENDED DC OPERATING CONDITIONS

(T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−0.5 *	—	.65	V
C_L	Output Load	—	—	100	pF
TTL	Output Load	—	—	1	—

*V_{IL} min = −1.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M864/8M864 MIN.	TYP.(1)	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{OE}$ or $\overline{CS_1} \geq V_{IH}$, or $CS_2 \leq V_{IL}$, V_{OUT} = 0V to V_{CC}	—	—	15	µA
I_{CC}	Operating Power Supply Current	$\overline{CS_1} \leq V_{IL}$, $CS_2 \geq V_{IH}$, Output Open	—	65	180	mA
I_{CC1}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	65	180	mA
I_{SB}	Standby Power Supply Current	$\overline{CS_1} \geq V_{IH}$, or $CS_2 \leq V_{IL}$	—	20	80	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS_1} \geq V_{CC} - 0.2V$, and/or $CS_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	—	.016	3.6(2)	mA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1mA	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C
2. I_{SB1} max at commercial temperature 1.0 mA

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−10 to +85	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	4.0	4.0	W
I_{OUT}	DC Output Current	50	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	10ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL Gate and C_L = 100pF (including scope and jig)

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

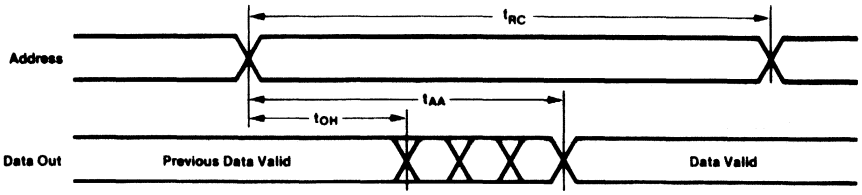
SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	28	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	33	pF

NOTE: This parameter is sampled and not 100% tested.

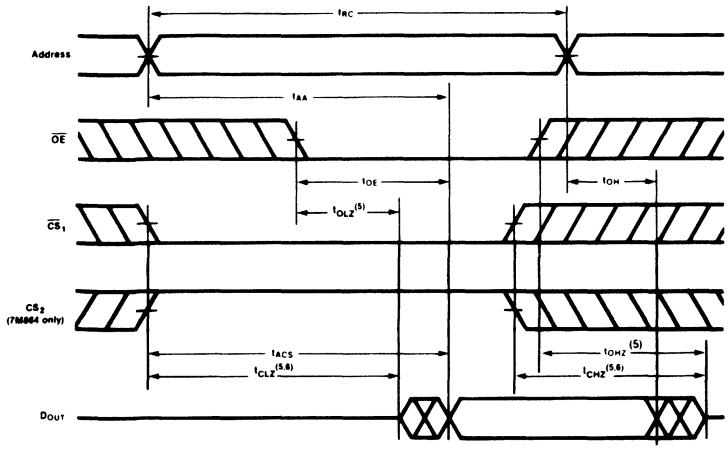
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	IDT7M/ 8M864L65 COMMERCIAL ONLY		IDT7M/ 8M864L75		IDT7M/ 8M864L85		IDT7M/ 8M864L120		IDT7M/ 8M864L150		IDT7M/ 8M864L200		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE														
t_{RC}	Read Cycle Time	65	—	75	—	85	—	120	—	150	—	200	—	ns
t_{AA}	Address Access Time	—	65	—	75	—	85	—	120	—	150	—	200	ns
t_{ACS}	Chip Select Access Time	—	65	—	75	—	85	—	120	—	150	—	200	ns
t_{CLZ}	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	50	—	55	—	65	—	65	—	80	—	100	ns
t_{OLZ}	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{CHZ}	Output Deselection to Output in High Z	—	40	—	50	—	55	—	70	—	70	—	80	ns
t_{OHZ}	Chip Disable to Output in High Z	—	30	—	35	—	40	—	40	—	40	—	50	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	0	—	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	65	—	75	—	85	—	120	—	150	—	200	—	ns
t_{CW}	Chip Selection to End of Write	55	—	65	—	65	—	80	—	100	—	120	—	ns
t_{AW}	Address Valid to End of Write	60	—	70	—	70	—	85	—	100	—	120	—	ns
t_{AS}	Address Setup Time	10	—	15	—	15	—	15	—	20	—	20	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	55	—	55	—	70	—	90	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	10	—	10	—	10	—	10	—	ns
t_{OHZ}	Output Disable to Output in High Z	—	30	—	35	—	40	—	40	—	40	—	50	ns
t_{WHZ}	Write to Output in High Z	0	35	0	40	0	50	0	50	0	60	0	60	ns
t_{DW}	Data to Write Time Overlap	25	—	30	—	30	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold from Write Time	5	—	10	—	10	—	10	—	10	—	10	—	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	5	—	ns

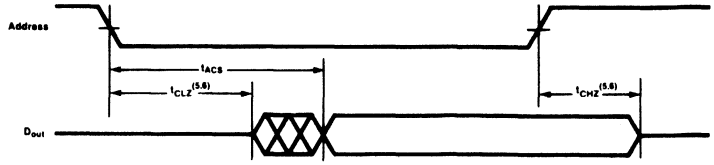
TIMING WAVEFORM OF READ CYCLE NO. 1 (1,2,4)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1,3)



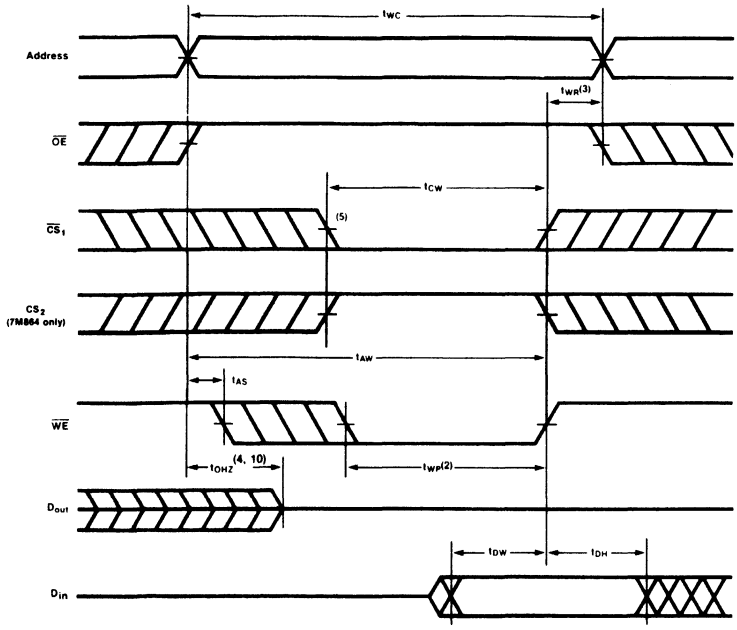
TIMING WAVEFORM OF READ CYCLE NO. 3 (1,3,4)



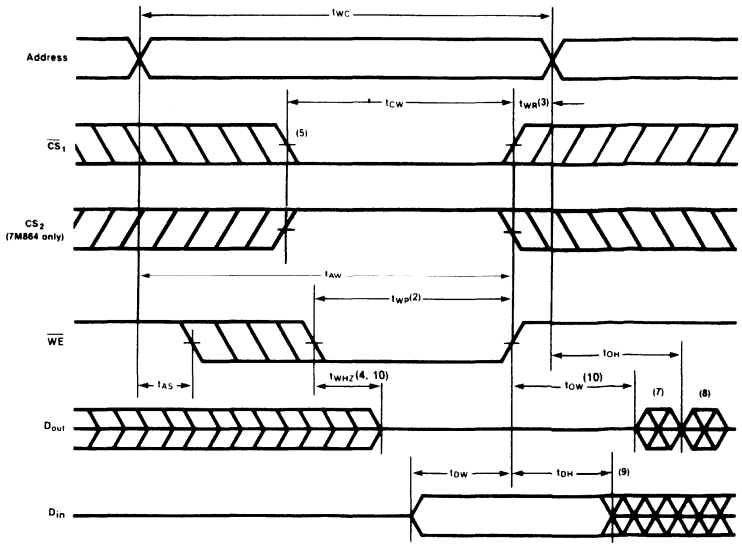
NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. Device is continuously selected, $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH} (7M864 only).
3. Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high (7M864 only).
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
6. For any given speed grade, operating voltage, and temperature, t_{CHZ} will be less than or equal to t_{CLZ}.

SUBSYSTEMS

TIMING WAVEFORMS OF WRITE CYCLE 1[1]



WRITE CYCLE 2[1,6]



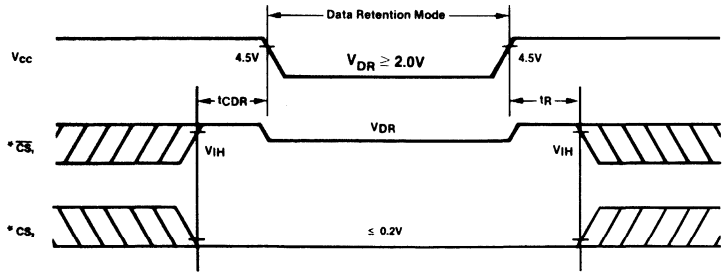
NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}_1$, or high CS_2 (7M864 only) and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}_1$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}_1$ low transition or CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continously low ($\overline{OE}$ = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}_1$ is low or CS_2 is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.[1]	MAX COMM.	MAX. MIL.	UNIT
V_{DR}	V_{CC} for Data Retention		2.0	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}_1 \geq V_{CC} - 0.2V$, $CS_2 \leq 0.2V$	—	2.0[2]	350[2]	1200[2]	µA
		$V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	—	4.0[3]	500[3]	1800[3]	
t_{CDR}	Chip Deselect to Data Retention Time		0	—	—	—	ns
t_R	Operation Recovery Time		t_{RC}[4]	—	—	—	ns

NOTES:
1. T_A = 25°C
2. at V_{CC} = 2.0V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time

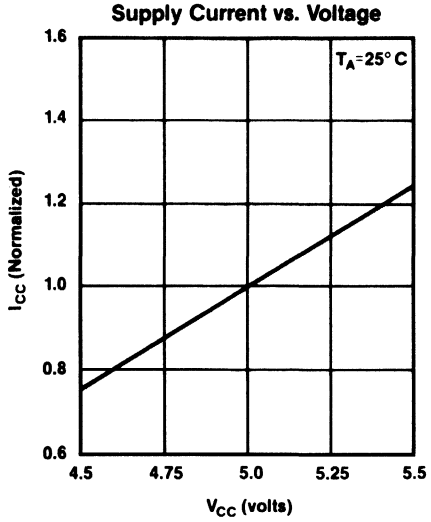
LOW V_{CC} DATA RETENTION WAVEFORM



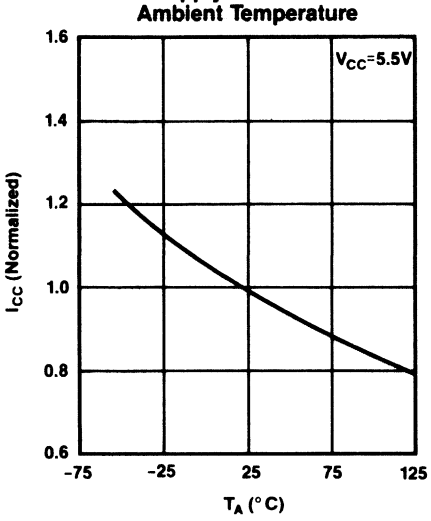
*Low V_{CC} data retention achieved by the indicated $\overline{CS}_1$ waveform or CS_2 waveform.

NORMALIZED TYPICAL PERFORMANCE CHARACTERISTICS

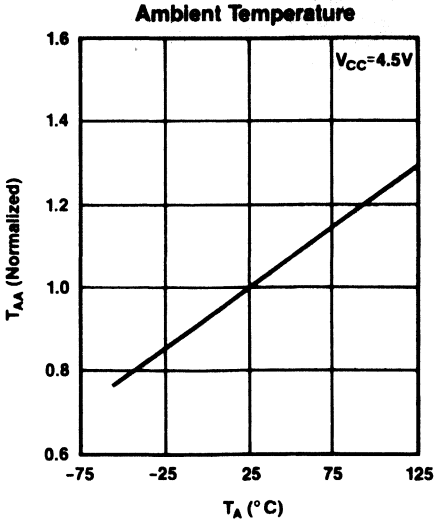
Supply Current vs. Voltage



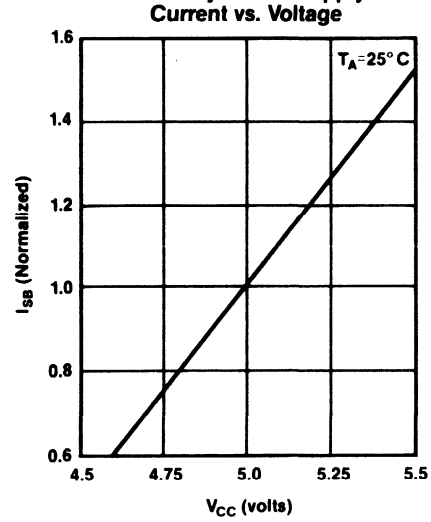
Supply Current vs. Ambient Temperature



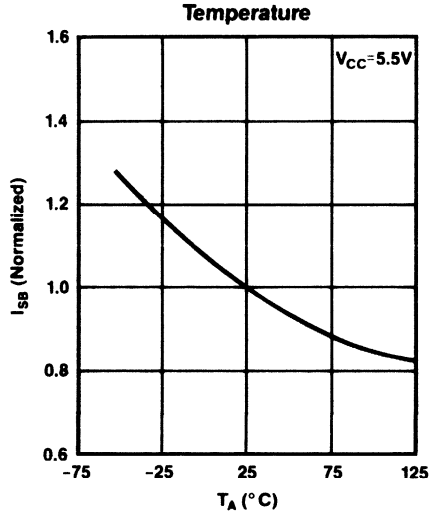
Address Access Time vs. Ambient Temperature



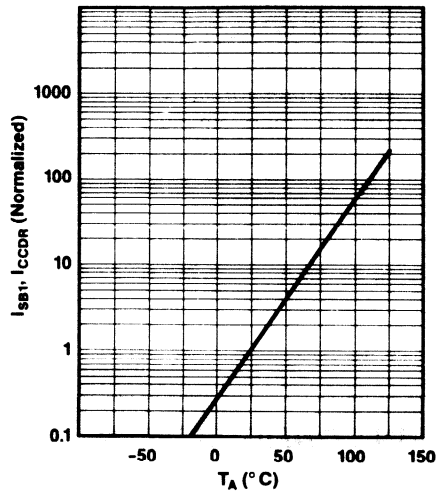
Stand-by Power Supply Current vs. Voltage



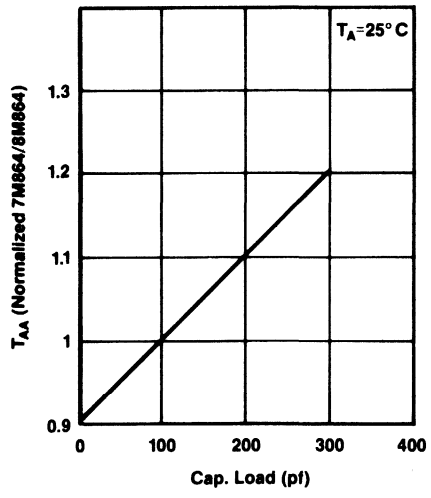
Stand-by Power Supply Current vs. Ambient Temperature



Full Stand-by Power Supply Current. Data Retention Current vs. Ambient Temperature



Address Access Time vs. Capacitive Load



SUBSYSTEMS

Integrated Device Technology, Inc.

256K (32K x 8 BIT) CMOS STATIC RAMPAK

PRELIMINARY
IDT7M856

FEATURES:

- High-density 256K (32K x 8) bit CMOS static RAM module
- Equivalent to JEDEC standard for future monolithic 32K x 8 static RAMs
- High-speed—60ns (max.) commercial; 75ns (max.) military
- Low power consumption; typically less than 1W operating, less than 500μW in standby
- Utilizes IDT7198s—high-performance 64K static RAMs produced with advanced CEMOS™ II technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in the JEDEC standard 28-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- RAMPAKs available with semiconductor components 100% screened to MIL-STD-883, Class B
- Finished RAMPAKs tested at Room, Hot and Cold temperatures for all AC and DC parameters as per customer requirements

DESCRIPTION:

The IDT7M856 is a 256K (32,768 x 8) bit high-speed static RAM constructed on a co-fired ceramic substrate using four IDT7198 (16,384 x 4) static RAMs in leadless chip carriers. Functional equivalence to proposed monolithic 256K static RAMs is achieved by utilization of an on-board decoder used as an inverter that interprets the higher order address A_{14} to select two of the four 16K x 4 RAMs. Extremely fast speeds can be achieved with this technique due to use of 64K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability technology, CEMOS II.

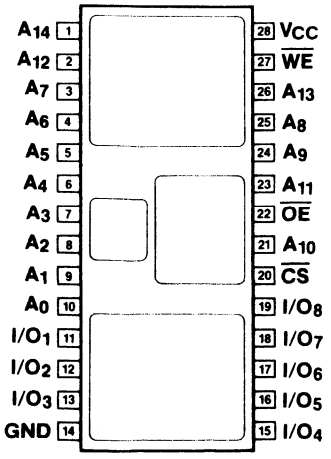
The IDT7M856 is available with maximum access times as fast as 60ns for commercial and 75ns for military temperature ranges, with maximum power consumption of only 2 watts. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to a standby mode with maximum power consumption of 990mW. Substantially lower power levels can be achieved in a full standby mode (66mW max.)

The IDT7M856 is offered in a 28-pin, 600 mil center sidebraze DIP. This provides four times the density of the IDT7M864 (8K x 8 module) in the same socket with only minor pin assignment changes. In addition, the JEDEC standards for 256K monolithic pinouts has been adhered to, allowing for compatibility with future monolithics.

All inputs and outputs of the IDT7M856 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used requiring no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

All IDT military RAMPAK semiconductor components are 100% processed to the test methods of MIL-STD-833, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

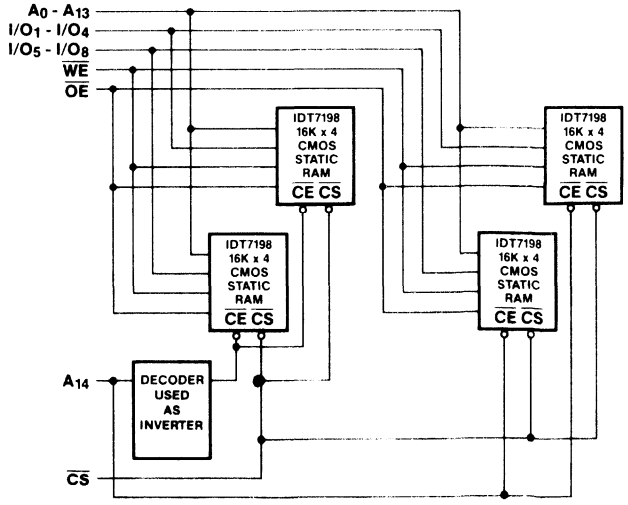
PIN CONFIGURATION



PIN NAMES

A_0 - A_{14}	ADDRESSES
I/O_1 - I/O_8	DATA INPUT/OUTPUT
$\overline{CS}$	CHIP SELECT
V_{CC}	POWER
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
GND	GROUND

FUNCTIONAL BLOCK DIAGRAM



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MILITARY AND COMMERCIAL TEMPERATURE RANGES

Printed in U.S.A.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
P_T	Power Dissipation	4.0	4.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} min = -3.0V pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open	—	190	360	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	190	360	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$	—	90	180	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or ≤ 0.2V	—	0.1	12.0	mA
V_{OL}	Output Low Voltage	I_{OL} = 10mA I_{OL} = 8mA	— —	— —	0.5 0.4	V V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	—	V

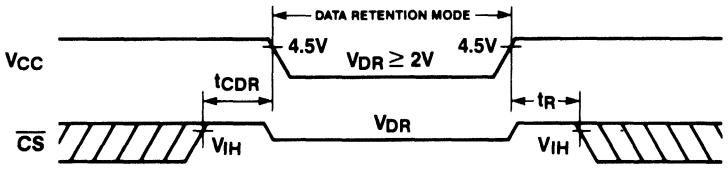
NOTE:
1. V_{CC} = 5V, T_A = +25°C

LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	COM'L MAX.	MIL MAX.	UNIT
V_{DR}	V_{CC} for Data Retention		2.0	–	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ -0.2V or ≤ 0.2V	— —	6.0(2) 12.0(3)	1000(2) 1500(3)	4000(2) 6000(3)	µA
t_{CDR}	Chip Deselect to Data Retention Time		0	—	—	—	ns
t_R	Operation Recovery Time		t_{RC}(4)	—	—	—	ns

NOTES:
1. T_A = +25°C
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM

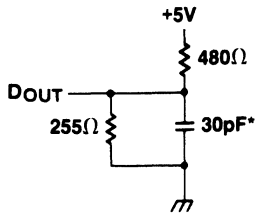


SRD7198S/L-012

SUBSYSTEMS

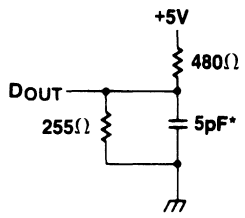
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2



SRD7198S/L-005

Figure 1. Output Load



SRD7198S/L-006

Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

***Including scope and jig**

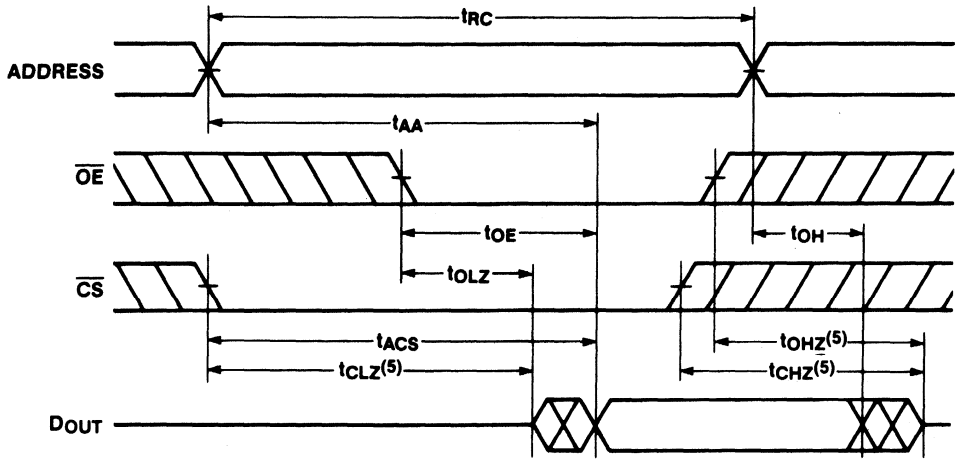
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7M856S60 MIN.	IDT7M856S60 MAX.	IDT7M856S70 MIN.	IDT7M856S70 MAX.	IDT7M856S85 MIN.	IDT7M856S85 MAX.	UNITS
READ CYCLE								
t_{RC}	Read Cycle Time	60	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	60	—	70	—	85	ns
t_{ACS}	Chip Select Access Time	—	60	—	70	—	85	ns
t_{CLZ}	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	40	—	45	—	55	ns
t_{OLZ}	Output Enable to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ}	Chip Select to Output in High Z	—	20	—	25	—	30	ns
t_{OHZ}	Output Disable to Output in High Z	—	20	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	ns
t_{PD}	Chip Deselection to Power Down Time	—	60	—	70	—	85	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	60	—	70	—	85	—	ns
t_{CW}	Chip Selection to End of Write	50	—	60	—	75	—	ns
t_{AW}	Address Valid to End of Write	50	—	60	—	75	—	ns
t_{AS}	Address Setup Time	10	—	10	—	15	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output High Z	—	25	—	30	—	40	ns
t_{DW}	Data to Write Time Overlap	25	—	30	—	40	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	ns
t_{OW}	Output Active from End of Write	5	—	5	—	5	—	ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7M856S75		IDT7M856S90		IDT7M856S100		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE								
t_{RC}	Read Cycle Time	75	—	90	—	100	—	ns
t_{AA}	Address Access Time	—	75	—	90	—	100	ns
t_{ACS}	Chip Select Access Time	—	65	—	80	—	90	ns
t_{CLZ}	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	50	—	60	—	65	ns
t_{OLZ}	Output Enable to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ}	Chip Select to Output in High Z	—	30	—	35	—	40	ns
t_{OHZ}	Output Disable to Output in High Z	—	30	—	35	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	ns
t_{PD}	Chip Deselection to Power Down Time	—	75	—	90	—	100	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	75	—	90	—	100	—	ns
t_{CW}	Chip Selection to End of Write	65	—	80	—	90	—	ns
t_{AW}	Address Valid to End of Write	65	—	80	—	90	—	ns
t_{AS}	Address Setup Time	10	—	15	—	20	—	ns
t_{WP}	Write Pulse Width	45	—	50	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output High Z	—	40	—	50	—	50	ns
t_{DW}	Data to Write Time Overlap	35	—	45	—	45	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	ns
t_{OW}	Output Active from End of Write	5	—	5	—	5	—	ns

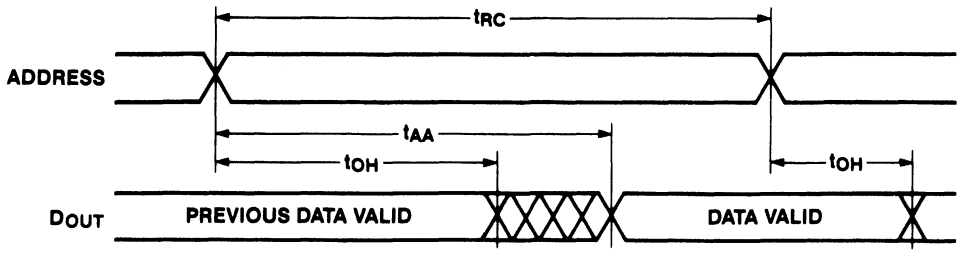
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



SRD7198S/L-007

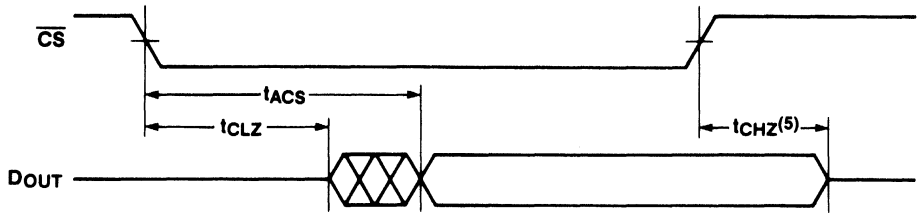
SUBSYSTEMS

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



SRD7198S/L-008

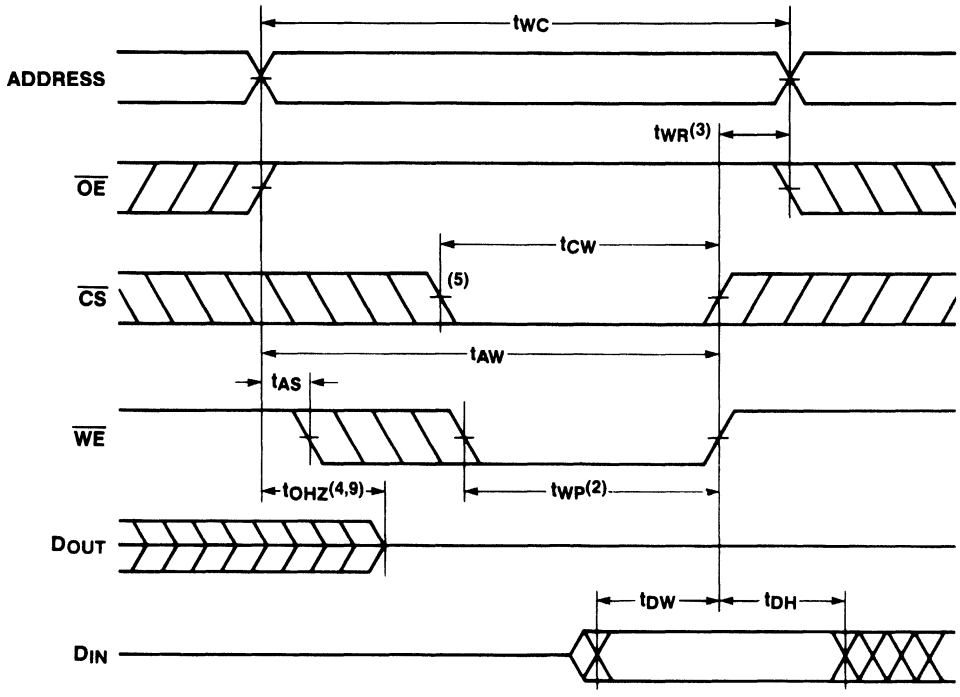
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



SRD7198S/L-009

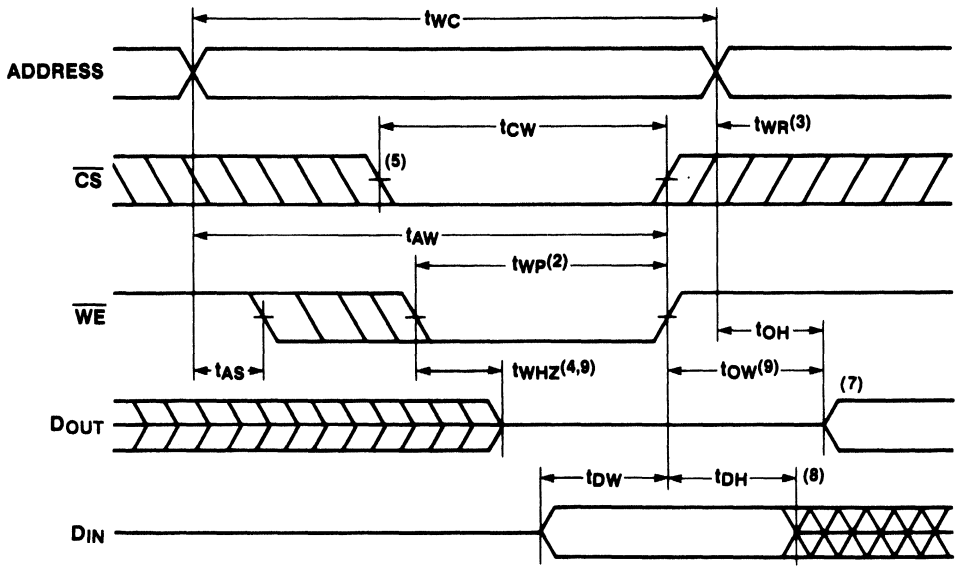
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



SRD7198S L-010

TIMING WAVEFORM OF WRITE CYCLE NO. 2(1,6)



SRD7198S/L-011

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	High Z	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High Z	Active
Write	L	X	L	D_{IN}	Active

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	26	pF

NOTE:
1. This parameter is sampled and not 100% tested.

SUBSYSTEMS

Integrated Device Technology, Inc.

256K CMOS STATIC RAMPAK

IDT7M656

FEATURES:

- High-density 256K-bit CMOS static RAM Module
- Customer-configured to 16Kx16, 32Kx8 or 64Kx4
- Fast access times
  —Commercial - 55ns
  —Military - 65ns
- Low power consumption
  —Active: 2W (typ.) (in 16Kx16 organization)
  —Standby: 0.16mW (typ.)
- Utilizes 16 IDT6167s - high-performance 16Kx1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high reliability vapor phase solder reflow process
- Offered in 40-pin, 900 mil center sidebraze DIP, achieving very high memory density
- Single 5V (±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- RAMPAKs available with components 100% screened to MIL-STD-883 Class B

DESCRIPTION:

The IDT7M656 is a 256K-bit high-speed CMOS static RAM constructed on a multilayered ceramic substrate using 16 IDT6167 (16Kx1) static RAMs in leadless chip carriers. Making 4 chip select lines available (one for each group of 4 RAMs) allows the user to configure the memory into a 16Kx16, 32Kx8 or 64Kx4 organization. In addition, extremely high speeds are achievable by the use of IDT6167s fabricated in IDT's high performance, high reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides some of the fastest 16K static RAMs available.

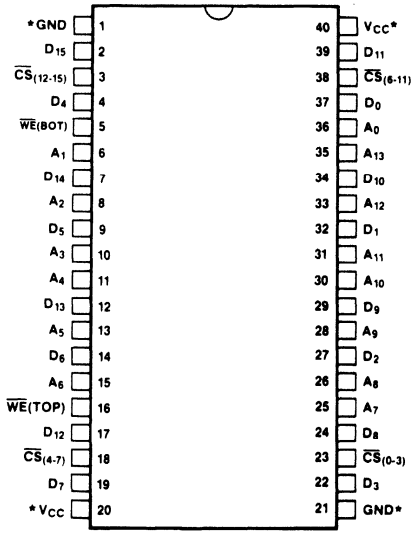
The IDT7M656 is available with access times as fast as 55ns commercial and 65ns military temperature range, with maximum operating power consumption of only 4.4W (significantly less if organized 32Kx8 or 64Kx4). The RAMPAK also offers a maximum standby power mode of 1.7W and a maximum full standby mode of 82.5mW.

The IDT7M656 is offered in a high-density 40-pin, 900 mil center sidebraze DIP to take full advantage of the compact IDT6167 in leadless chip carriers.

All inputs and outputs of the IDT7M656 are TTL-compatible and operate from a single 5V supply. (NOTE: Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.) Full asyncronous circuitry is used requiring no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

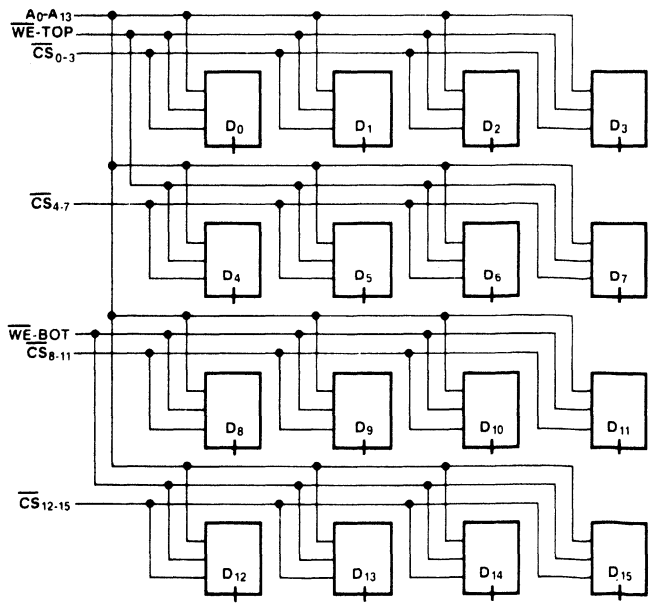
All IDT military RAMPAK components are 100% processed to the test methods of MIL-STD-883 Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



* Both V_{CC} pins need to be connected to the 5V Supply, and both GND pins need to be grounded for proper operation.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

Axx	ADDRESSES	Dxx	DATA IN/OUT
$\overline{CS}$xx	CHIP SELECTS	Vcc	POWER
$\overline{WE}$xx	WRITE ENABLES	GND	GROUND

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TRUTH TABLE

MODE	$\overline{CS}_{XX}$	$\overline{WE}_{XX}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} min = -1.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M656 MIN.	IDT7M656 TYP.(1)	IDT7M656 MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}_{XX}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	20	µA
I_{CCX16}	Operating Current in X16 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, Min. Duty Cycle = 100%	—	400	800	mA
I_{CCX8}	Operating Current in X8 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, Min. Duty Cycle = 100%	—	240	560	mA
I_{CCX4}	Operating Current in X4 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, Min. Duty Cycle = 100%	—	160	440	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}_{XX} \geq V_{IH}$	—	80	320	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}_{XX} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or ≤ 0.2V	—	.032	15(2)	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	—	V

NOTES:
1. V_{CC} = 5V, T_A = 25°C
2. I_{SB1} max. at commercial temperature = 5.0mA

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	8.0	8.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

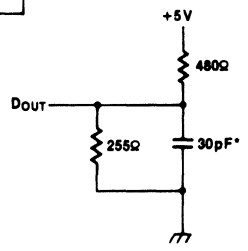


Figure 1. Output Load

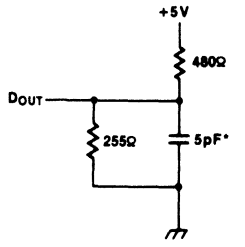


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

*Including scope and jig.

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	200	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	60	pF

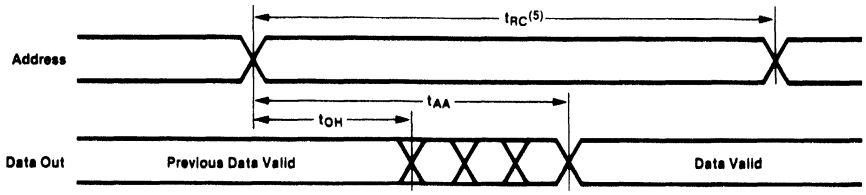
NOTE:
This parameter is sampled and not 100% tested

SUBSYSTEMS

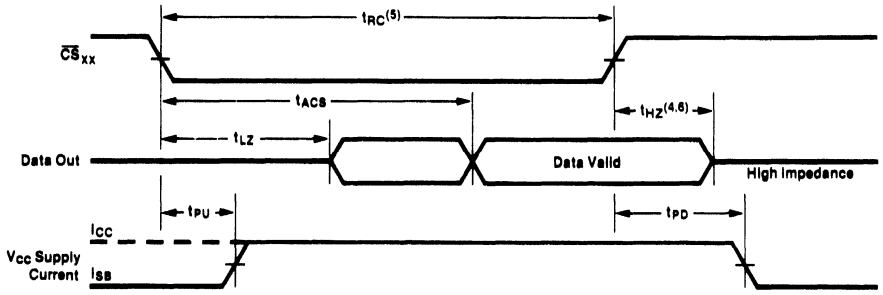
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	IDT7M656L55 COMMERCIAL ONLY MIN.	MAX.	IDT7M656L65 MIN.	MAX.	IDT7M656L85 MIN.	MAX.	IDT7M656L100 MILITARY ONLY MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	55	—	65	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	65	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	55	—	65	—	85	—	100	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{LZ}	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{HZ}	Chip Deselection to Output in High Z	0	40	0	40	0	50	0	50	ns
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselection to Power Down Time	—	55	—	65	—	85	—	100	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	55	—	65	—	85	—	100	—	ns
t_{CW}	Chip Selection to End of Write	45	—	55	—	65	—	80	—	ns
t_{AW}	Address Valid to End of Write	45	—	55	—	65	—	80	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	35	—	40	—	45	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	25	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High Z	0	40	0	40	0	50	0	50	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

TIMING WAVEFORM OF READ CYCLE NO. 1(1,2)



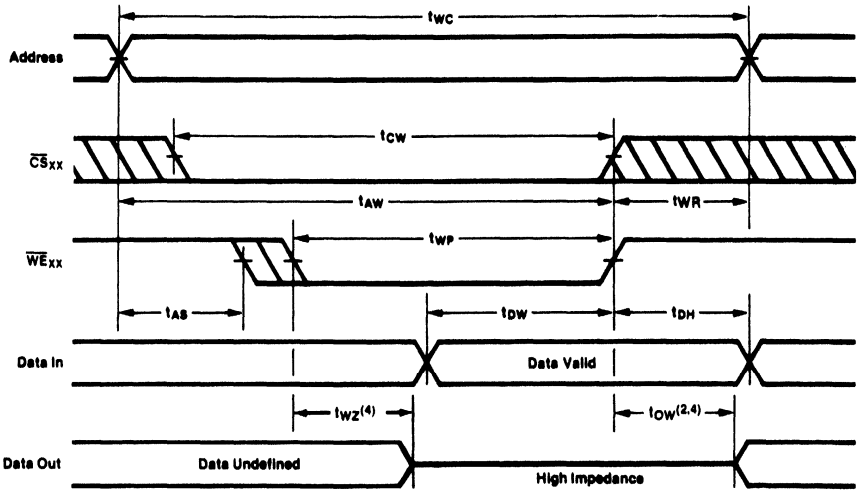
TIMING WAVEFORM OF READ CYCLE NO. 2(1,3)



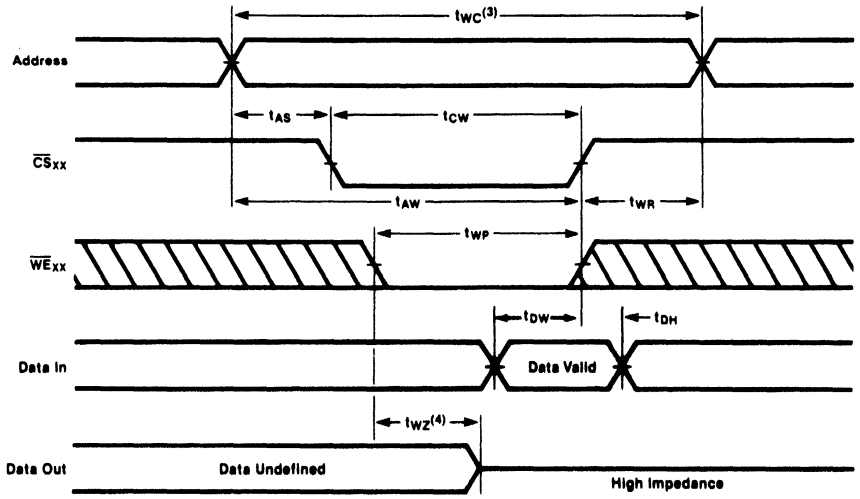
NOTES:

1. $\overline{WE}_{XX}$ is high for READ cycle.
2. $\overline{CS}_{XX}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}_{XX}$ transition low.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. For any given speed grade, operating voltage, and temperature, t_{HZ} will be less than or equal to t_{LZ}.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (CS CONTROLLED)(1)



NOTES:

1. $\overline{CS}_{XX}$ or $\overline{WE}_{XX}$ must be high during address transitions.
2. If $\overline{CS}_{XX}$ goes high simultaneously with $\overline{WE}_{XX}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.

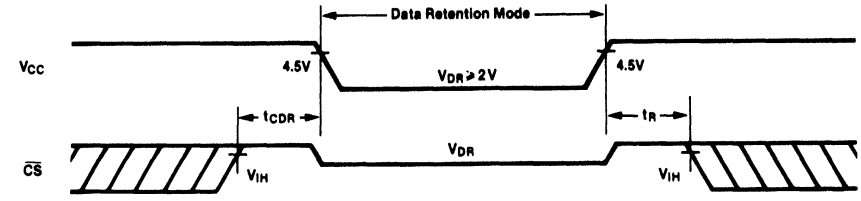
LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.(1)	MAX COMM.	MAX. MIL.	UNIT
V_{DR}	V_{CC} for Data Retention		2.0	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}_{XX} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $\leq$ 0.2V	— —	.01(2) .02(3)	2.0(2) 3.0(3)	6.0 9.0	mA
t_{CDR}	Chip Deselect to Data Retention Time		0	—	—	—	ns
t_R	Operation Recovery Time		t_{RC}(4)	—	—	—	ns

NOTES:

1. T_A = 25°C
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time

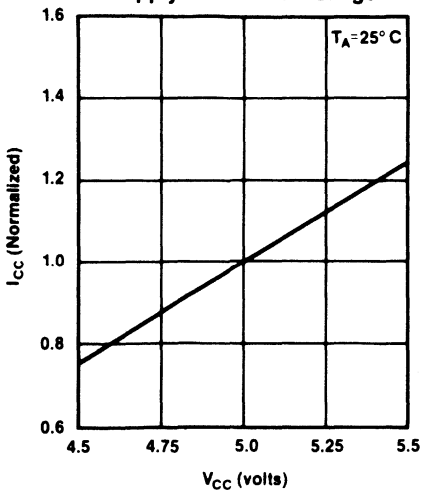
LOW V_{CC} DATA RETENTION WAVEFORM



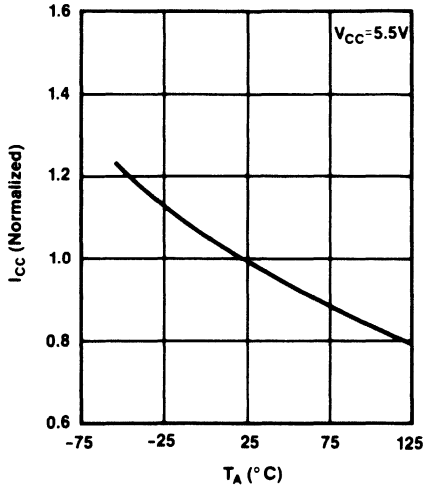
SUBSYSTEMS

NORMALIZED TYPICAL PERFORMANCE CHARACTERISTICS

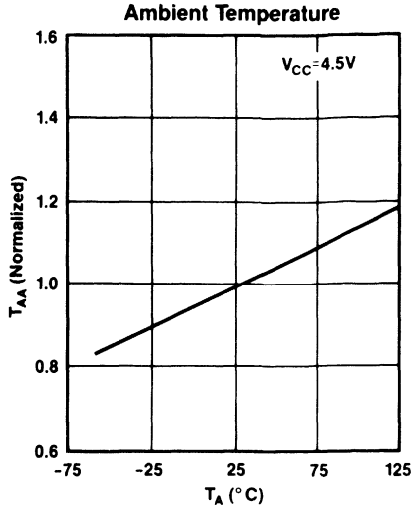
Supply Current vs. Voltage



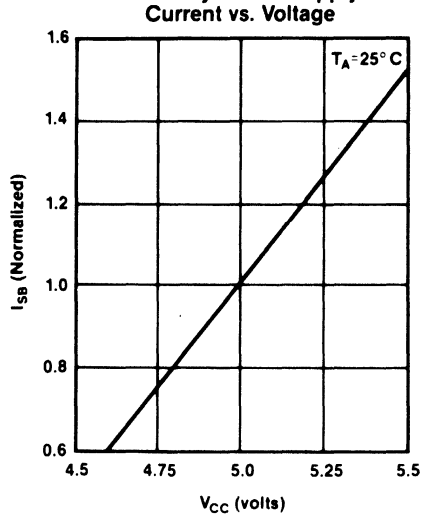
Supply Current vs. Ambient Temperature



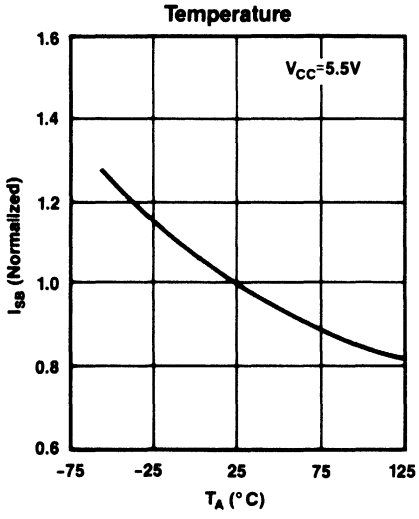
Address Access Time vs. Ambient Temperature



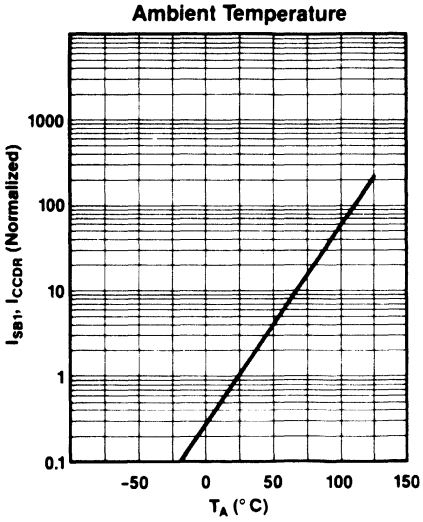
Stand-by Power Supply Current vs. Voltage



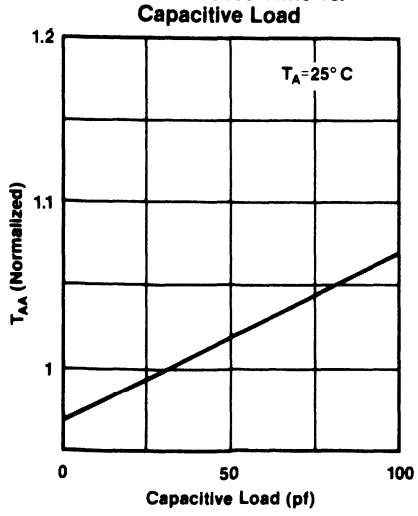
Stand-by-Power Supply Current vs. Ambient Temperature



Full Stand-by Power Supply Current. Data Retention Current vs. Ambient Temperature

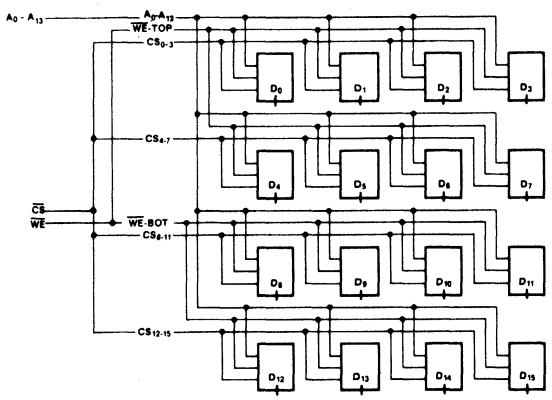


Address Access Time vs. Capacitive Load



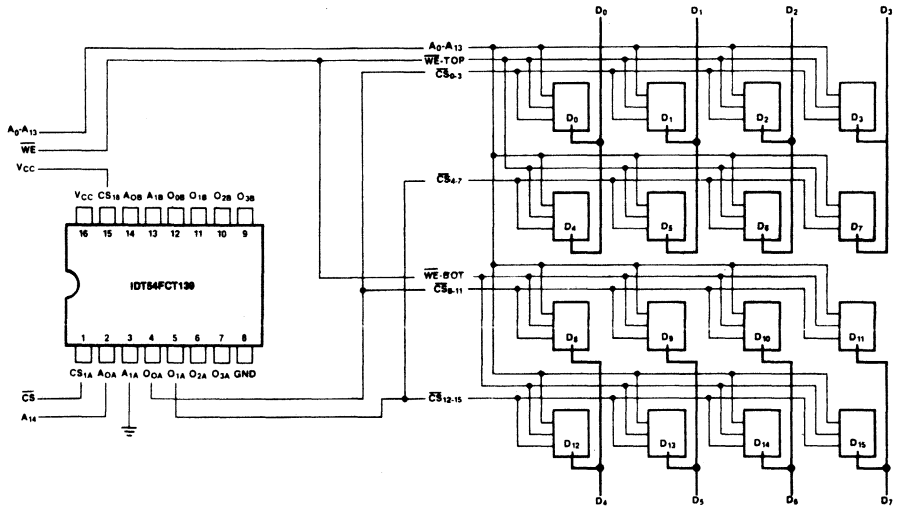
IDT7M656

16K x 16 CONFIGURATION



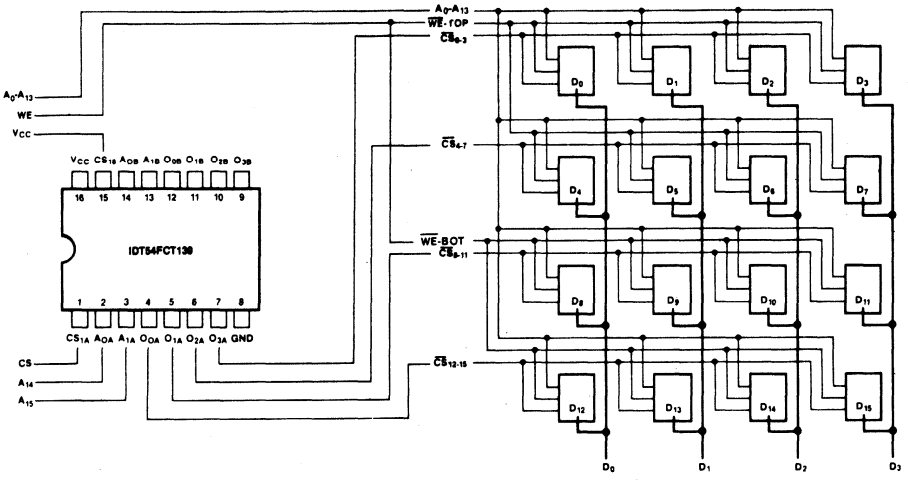
NOTES:
1. All chip selects tied together since, in a by 16 configuration, all chips are either on or off.
2. The two write enables are tied together allowing control of the write enable for entire memory at one time (necessary) in a by 16 organization since all chips are either writing or reading at any given time.

32K x 8 CONFIGURATION



NOTES:
1. The chip selects are tied together in groups of two. The decoder uses the new higher order address pin (A_{14}) to determine which of the two banks of memory are enabled.
2. The two write enables are tied together for ease of layout. They could be controlled by the decoder similar to the chip selects but would save only a minimal amount of power and add complexity to the layout.

64K x 4 CONFIGURATION



NOTES:
1. Each chip select is now controlled by the two higher order address pins A_{14} (necessary in 64K deep memory).
2. Again the two write enables are tied together for ease of layout (the megabit part will only have one write enable pin).

SUBSYSTEMS

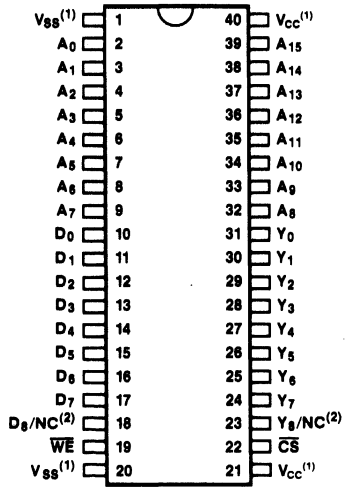
512K CMOS STATIC 64Kx8 or 64Kx9 RAMPAK

ADVANCE INFORMATION
IDT7M812
IDT7M912

FEATURES

- High-density 512K-bit CMOS static RAM module
- 64Kx8 (IDT7M812) or 64Kx9 (IDT7M912) configuration
- Fast access times
  - —Military: 70ns (max.)
  - —Commercial: 60ns (max.)
- Low power consumption
  - —Active: 1.8W (typ. in 64Kx8 organization)
  - —Standby: 240μW (typ. in 64Kx8 organization)
- Utilizes 8 (IDT7M812) or 9 (IDT7M912) IDT7187 high-performance 64Kx1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Available in 40-pin, 600 mil center sidebraze DIP, achieving very high memory density
- Single 5V (±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- RAMPAKs available with semiconductor components 100% screened to MIL-STD-883, Class B
- Finished military RAMPAKs tested at Room, Hot and Cold temperatures for all AC and DC parameters

PIN CONFIGURATION



SSD7M812-001

DIP
TOP VIEW

NOTES

1. Both V_{CC} pins need to be connected to the 5V supply, and both GND pins need to be grounded for proper operation.
2. Pin 18 is D_8 and pin 23 is Y_8 in 64Kx9 (IDTM912) option, and both 18 and 23 are NC in 64Kx8 (IDT7M812) option.

DESCRIPTION:

The IDT7M812/IDT7M912 are 512K-bit high-speed CMOS static RAMs constructed on a multi-layered ceramic substrate using 8 IDT7187 64Kx1 static RAMs (IDT7M812) or 9 IDT7187 static RAMs (IDT7M912) in leadless chip carriers. Extremely high speeds are achievable by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 64K static RAMs available.

The IDT7M812/IDT7M912 are available with access times as fast as 60ns commercial and 70ns military temperature range, with maximum operating power consumption of only 2.5W (IDTM912, 64Kx9 option). The RAMPAK also offers a maximum standby power mode of less than 1W and a maximum full standby mode of 45mW.

The IDT7M812/IDT7M912 are offered in a high-density 40-pin, 600 mil center sidebraze DIP to take full advantage of the compact IDT7187s in leadless chip carriers. The IDT7M912 (64Kx9) option can provide more flexibility in system application for error detection, parity bit, etc.

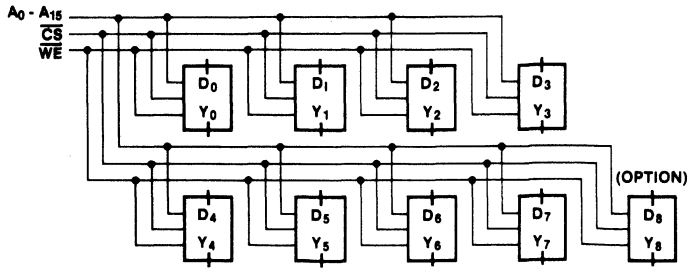
All inputs and outputs of the IDT7M812/IDT7M912 are TTL-compatible and operate from a single 5V supply. (Note: Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation). Fully asynchronous circuitry is used requiring no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

All IDT military RAMPAK semiconductor components are 100% processed to the test methods of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance reliability.

PIN NAMES

A_0 - A_{15}	ADDRESS
D_0 - D_8	DATA INPUT
Y_0 - Y_8	DATA OUTPUT
$\overline{CS}$	CHIP SELECT
$\overline{WE}$	WRITE ENABLE
V_{CC}	POWER
GND	GROUND

FUNCTIONAL BLOCK DIAGRAM



SSD7M812-002

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1 MEGABIT CMOS STATIC RAMPAK

ADVANCE INFORMATION
IDT7M624

FEATURES:

- High density 1024K-bit CMOS static RAM module
- Customer-configured to 64K x 16, 128K x 8 or 256K x 4
- Fast access times
  - — Military: 70ns (max.)
  - — Commercial: 60ns (max.)
- Low power consumption
  - — Active: 2W (typ. in 64K x 16 organization)
  - — Standby: .160μW (typ.)
- Utilizes 16 IDT7187 high-performance 64K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in 40-pin, 900 mil center sidebraze DIP, achieving very high memory density
- Pin compatible with IDT7M656 (256K RAM module)
- Single 5V (±10%) power supply
- Dual GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- RAMPAKs available with semiconductor components 100% screened to MIL-STD-883, Class B
- Finished RAMPAKs tested at Room, Hot and Cold temperatures for all AC and DC parameters as per customer requirements

DESCRIPTION:

The IDT7M624 is a 1024K-bit high-speed CMOS static RAM constructed on a multi-layered ceramic substrate using 16 IDT7187 (64K x 1) static RAMs in leadless chip carriers. Making four chip select lines available (one for each group of 4 RAMs) allows the user to configure the memory into a 64K x 16, 128K x 8 or 256K x 4 organization. In addition, extremely high speeds are achievable by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 64K static RAMs available.

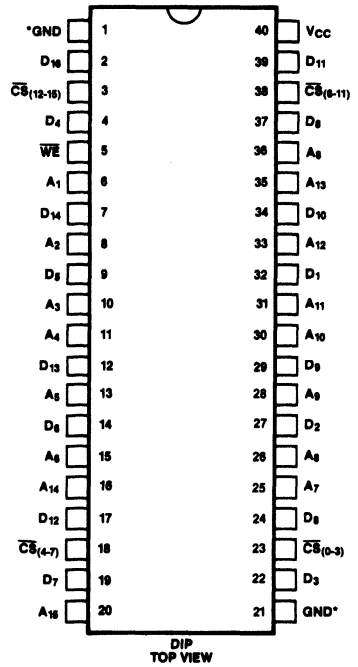
The IDT7M624 is available with access times as fast as 60ns commercial and 70ns military temperature range, with maximum operating power consumption of only 4.4W (significantly less if organized 128K x 8 or 256K x 4). The RAMPAK also offers a maximum standby power mode of 1.7W and a maximum full standby mode of 80mW.

The IDT7M624 is offered in a high-density 40-pin, 900 mil center sidebraze DIP to take full advantage of the compact IDT7187s in leadless chip carriers.

All inputs and outputs of the IDT7M624 are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used requiring no clocks or refreshing for operation, and provides equal access times for ease of use.

All IDT military RAMPAK semiconductor components are 100% processed to the test methods of MIL-STD-883 Class B, making them ideally suited to applications demanding the highest level of performance reliability.

PIN CONFIGURATION



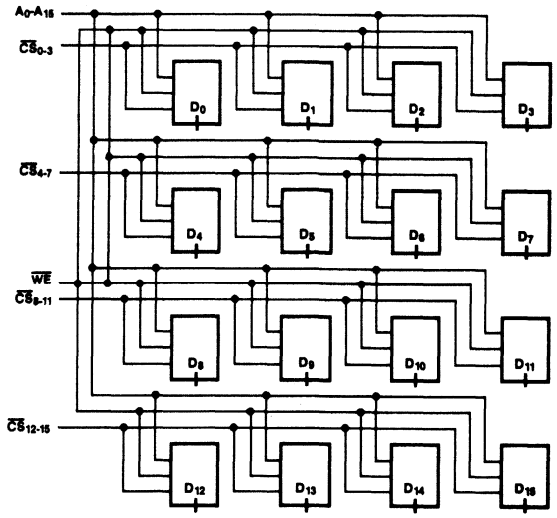
DIP
TOP VIEW

*Both GND Pins Need to Be Grounded for Proper Operation

PIN NAMES

A_0 - A_{15}	ADDRESSES
D_0 - D_{15}	DATA INPUT/OUTPUT
$\overline{CS}_{XX}$	CHIP SELECTS
$\overline{WE}$	WRITE ENABLE
V_{CC}	POWER
GND	GROUND

FUNCTIONAL BLOCK DIAGRAM



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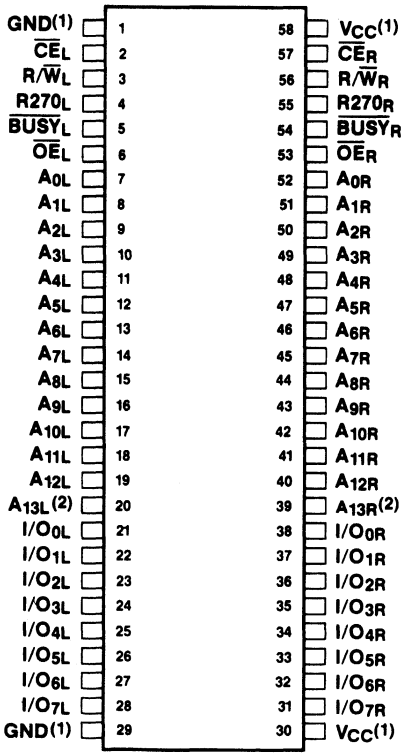
CMOS DUAL PORT RAM MODULE 64K (8Kx8) & 128K (16Kx8-BIT)

ADVANCE INFORMATION
IDT7M134
IDT7M135

FEATURES:

- High-density 64K/128K-bit CMOS dual port module
- 16Kx8 organization (IDT7M135) with 8Kx8 option (IDT7M134)
- Low power consumption
- CEMOS™ II process virtually eliminates alpha particle induced soft errors (with no organic die coating)
- On-chip port arbitration logic
- $\overline{BUSY}$ flags
- Fully asynchronous operation from either port
- Single 5V (±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- On-chip pull up resistors for open-drain $\overline{BUSY}$ flags option
- Inputs and output directly TTL-compatible
- Fully static operation
- Modules available with semiconductor components 100% screened to MIL-STD-883, Class B
- Finished military RAMPAKs tested at Room, Hot and Cold temperatures for all AC and DC parameters

PIN CONFIGURATION



NOTES
1. Both V_{CC} pins need to be connected to the 5V supply, and both GND pins need to be grounded for proper operation.
2. On 8Kx8 IDT7M134 option, A_{13L} and A_{13R} need to be externally connected to ground for proper operation.

DESCRIPTION:

The IDT7M134/135 are 64K/128K-bit high-speed CMOS dual port static RAM modules constructed on a multi-layered ceramic substrate using four IDT7132 2Kx8 dual port RAMs (IDT7M134) or eight IDT7132 dual port RAMs (IDT7M135) in leadless chip carriers. Dual port function is achieved by utilization of the two on-board IDT54/74FCT138 decoder circuits that interpret the higher order addresses A_{L11-13} and A_{R11-13} to select one of the eight 2Kx8 dual port RAMs. (On IDT7M134 8Kx8 option, the A_{L13} and A_{R13} need to be externally grounded and the selection becomes one of the four 2Kx8 dual port RAMs.) Extremely high speeds are achieved in this fashion due to the use of the IDT7132 dual port RAM, fabricated in IDT's high-performance CEMOS™ II technology.

The IDT7M134/IDT7M135 provide two ports with separate controls, address and I/O that permit independent access for reads or writes to any location in the memory. The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. The on-chip arbitration logic will determine which port has access and sets the $\overline{BUSY}$ flag of the delayed port. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. The delayed port will have access when $\overline{BUSY}$ goes high (inactive).

The IDT7M134/135 are available with access times as fast as 115ns commercial and 125ns military temperature range, with maximum operating power consumption of only 2.6W. The module also offers a maximum standby power mode of 1.9W and a maximum full standby mode of 440mW.

All IDT military module semiconductor components are 100% processed to the test methods of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	CHIP ENABLE
R/$\overline{W}_L$	R/$\overline{W}_R$	READ/WRITE ENABLE
$\overline{OE}_L$	$\overline{OE}_R$	OUTPUT ENABLE
$\overline{BUSY}_L$	$\overline{BUSY}_R$	$\overline{BUSY}$ FLAG
$R270_L$	$R270_R$	PULL-UP RESISTORS for Open-drain $\overline{BUSY}$ FLAG option
A_{0L}-A_{13L}	A_{0R}-A_{13R}	ADDRESS
I/O_{0L}-I/O_{7L}	I/O_{0R}-I/O_{7R}	DATA INPUT/OUTPUT
V_{CC}		POWER
GND		GROUND

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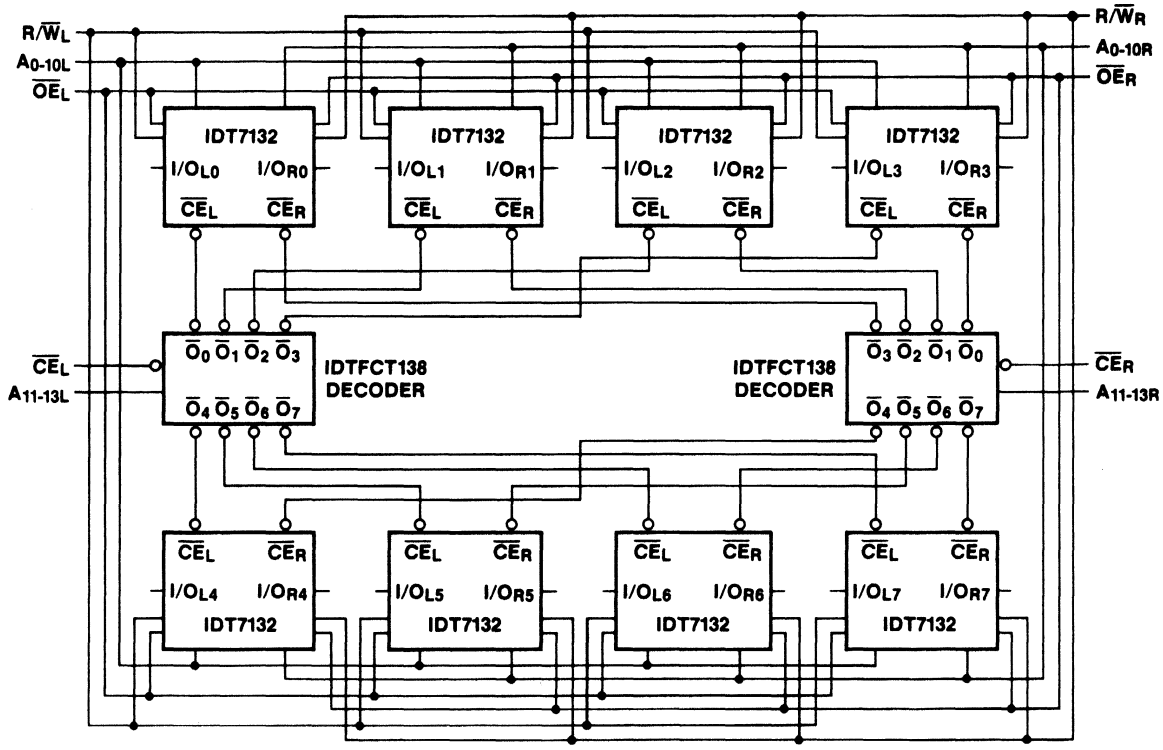
FUNCTIONAL BLOCK DIAGRAM



SUBSYSTEMS

CMOS PARALLEL IN-OUT FIFO MODULE 2Kx9-BIT & 4Kx9-BIT

PRELIMINARY
IDT7M203
IDT7M204

FEATURES:

- First-In, First-Out memory module
- 2Kx9 organization (IDT7M203)
- 4Kx9 organization (IDT7M204)
- Low power consumption
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Single 5V (±10%) power supply
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- High-performance CEMOS™II technology
- Pin compatible with Mostek MK4501 and IDT7201, but with four times word depth (IDT7M203) or eight times (IDT7M204)
- Module available with semiconductor components 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7M203/204 are FIFO memory modules that utilize a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. The device uses full and empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

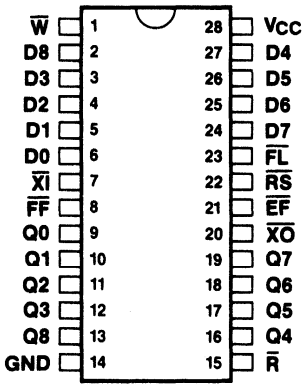
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The device has a read/write cycle time of 85ns (12MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

The IDT7M203/204 are constructed on a multi-layered ceramic substrate using four IDT7201 (512x9) or four IDT7202 (1Kx9) FIFOs in leadless chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7201s and IDT7202s fabricated in IDT's high-performance 2 micron technology, CEMOS II.

IDT's military FIFO modules have semiconductor components 100% processed to the test methods of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



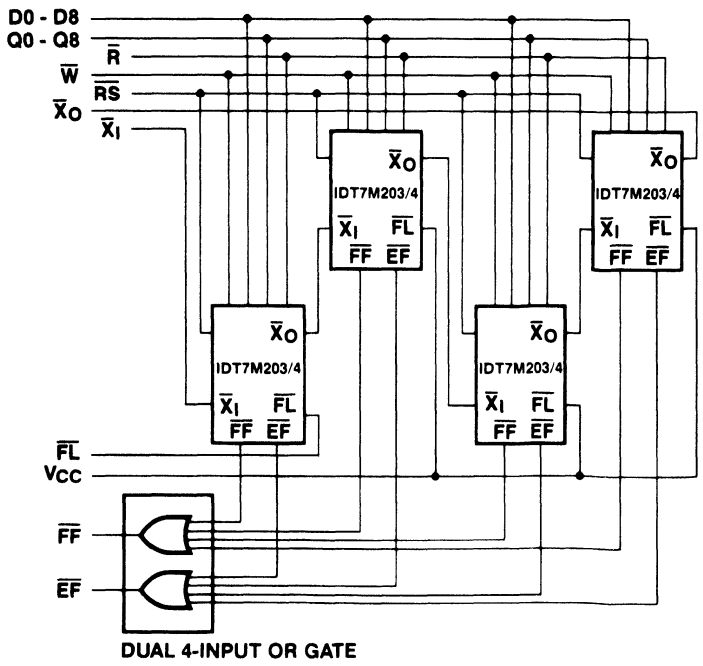
SSD7M203-001

DIP
TOP VIEW

PIN NAMES

$\overline{W}$ = WRITE	$\overline{FL}$ = FIRST LOAD	$\overline{XI}$ = EXPANSION IN	$\overline{EF}$ = EMPTY FLAG
$\overline{R}$ = READ	D = DATA IN	$\overline{XO}$ = EXPANSION OUT	V_{CC} = 5V
$\overline{RS}$ = RESET	Q = DATA OUT	$\overline{FF}$ = FULL FLAG	GND = GROUND

FUNCTIONAL BLOCK DIAGRAM



DUAL 4-INPUT OR GATE

SSD7M203-002

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85°	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
P_T	Power Dissipation	4.0	4.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V	—
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V	—
GND	Supply Voltage	0	0	0	V	—
V_{IH}	Input High Voltage Commercial	2.0	—	—	V	1
V_{IH}	Input High Voltage Military	2.2	—	—	V	—
V_{IL}	Input Low Voltage Commercial & Military	—	—	0.8	V	1

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

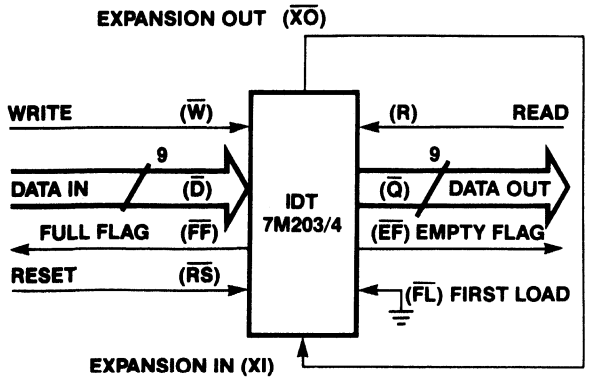
SYMBOL	PARAMETER	IDT7201S/L IDT7202S/L COMMERCIAL			IDT7201S/L IDT7202S/L MILITARY			UNIT	NOTES
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
I_{IL}	Input Leakage Current (Any Input)	-5	—	5	-10	—	10	μA	1
I_{OL}	Output Leakage Current	-10	—	10	-10	—	10	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1mA	2.4	--	—	2.4	—	—	V	—
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA	—	—	0.4	—	—	0.4	V	—
I_{CC1}	Average V_{CC} Power Supply Current	—	—	176	—	—	230	mA	3
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL}/\overline{RT}$ = V_{IH})	—	—	33	—	—	60	mA	3
$I_{CC3}(L)$	Power Down Current (All Input = V_{CC} -0.2V)	—	—	2.5	—	—	4.0	mA	3

NOTES:
1. Measurements with $0.4 \leq V_{IN} \leq V_{OUT}$.
2. $R \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$.
3. I_{CC} measurements are made with outputs open.

SUBSYSTEMS

OPERATING MODES: SINGLE DEVICE MODE

A single IDT7M203/IDT7M204 may be used when the application requirements are for 2048/4096 words or less. The IDT7M203/IDT204 is in a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is connected to the EXPANSION OUT ($\overline{XO}$) of the device and the FIRST LOAD ($\overline{FL}$) control pin is grounded (See Figure 8).



SSD7M203-010

Figure 8. Block Diagram of Single IDT7M203/IDT7M204 FIFO

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 9 demonstrates an 18-bit word width by using two IDT7M203/IDT7M204s. Any word width can be attained by adding additional IDT7M203/IDT7M204s.

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7M203/IDT7M204 can easily be adapted to applications when the requirements are for greater than 2048/4096 words. Figure 10 demonstrates Depth Expansion using three IDT7M203/IDT7M204s. Any depth can be attained by adding additional IDT7M203/IDT7M204s. The IDT7M203/IDT7M204 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the FIRST LOAD ($\overline{FL}$) control input.
2. All other device must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN (XI) pin of the next device. See Figure 10.
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s. (I.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 10.
5. The RETRANSMIT ($\overline{RT}$) function and HALF FULL FLAG ($\overline{HF}$) are not available in the Module application.

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays. (See Figure 11.)

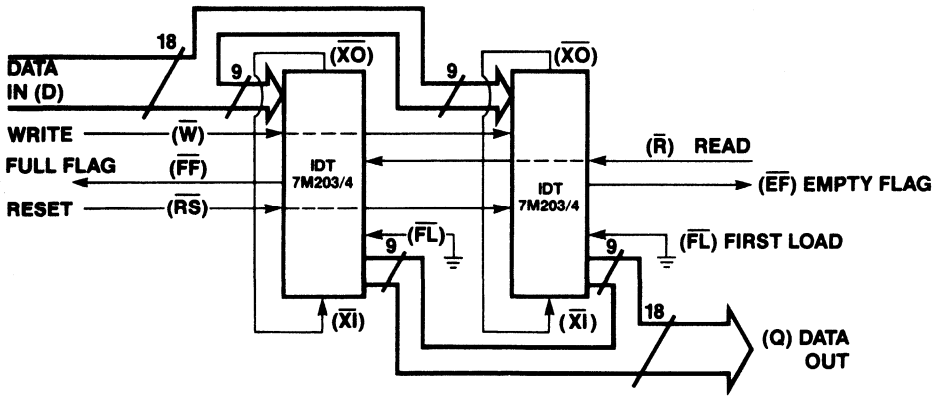
BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by pairing IDT7M203/IDT7M204s as is shown in Figure 12. Care must be taken to assure that the appropriate flag is monitored by each system. (I.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used.) Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW THRU MODES

Two types of flow through modes are permitted with the IDT7M203/IDT7M204: A read flow through and write flow through mode. For the read flow through mode (Figure 13), the FIFO permits a reading of a single word of data immediately after writing one word of data into the completely empty FIFO.

In the write flow through mode (Figure 14), the FIFO permits a writing of a single word of data immediately after reading one word of data from a completely full FIFO.



SSD7M203-011

NOTES:
Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 9. Block Diagram of 2048x18/4096x18 FIFO Memory Used in Width Expansion Mode

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D0 - D8)

Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the RESET ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) inputs must be in the high state during reset. HALF FULL FLAG ($\overline{HF}$) will be reset to high after master RESET ($\overline{RS}$).

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the FULL FLAG ($\overline{FF}$) is not set. Data setup and hold times must be adhered to with respect to the rising edge of the WRITE ENABLE ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

To prevent data overflow, the FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the FULL FLAG ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the READ ENABLE ($\overline{R}$) provided the EMPTY FLAG ($\overline{EF}$) is not set. The data is accessed on a First-In, First-Out basis independent of any ongoing write operations. After READ ENABLE ($\overline{R}$) goes high, the Data Outputs (Q0 through Q8) will return to a high impedance condition until the next READ operation. When all the data has been read from the FIFO, the EMPTY FLAG ($\overline{EF}$) will go low, inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the EMPTY FLAG ($\overline{EF}$) will go high after t_{WEF}, and a valid READ can then begin.

FIRST LOAD ($\overline{FL}$)

This pin is grounded to indicate that it is the first device. In the multiple module (depth expansion mode) application, this pin of the rest of devices should connect to V_{CC} for proper operation.

EXPANSION IN ($\overline{XI}$)

EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous (in depth expansion) or same device for proper application.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

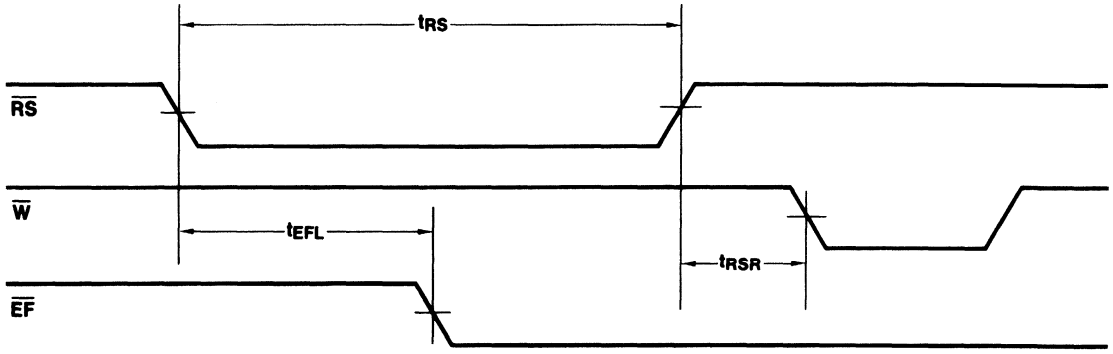
The FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location from the read pointer, indicating that the device is full. If the read pointer is not moved after RESET ($\overline{RS}$), the FULL FLAG ($\overline{FF}$) will go low after 2048 writes for the IDT7M203 and 4096 writes for the IDT7M204.

EXPANSION OUT ($\overline{XO}$)

EXPANSION OUT (XO) is connected to the EXPANSION IN ($\overline{XI}$) of the same device (single device mode) or the EXPANSION IN ($\overline{XI}$) of the first device (multiple device, depth expansion mode) for proper operation. This output acts as a signal to the first device by providing a pulse to the first device when the current device reaches the last location of memory.

DATA OUTPUTS (Q0 - Q8)

Data outputs for 9-bit wide data. This output is in a high impedance condition whenever READ ($\overline{R}$) is in a high state.



NOTES:
1. $t_{RSC} = t_{RS} + t_{RSR}$.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} during RESET.

Figure 2. Reset

SSD7M203-004

SUBSYSTEMS

CAPACITANCE (T_A = +25°C, f = 1.0MHz)[1]

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT	NOTES
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF	—
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF	1

NOTES:
1. This parameter is sampled and not 100% tested.

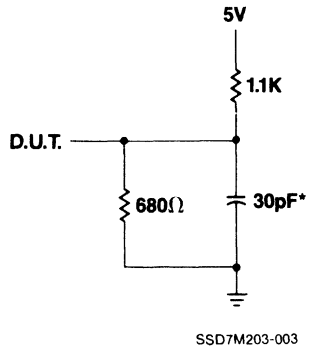
AC ELECTRICAL CHARACTERISTICS[1] (Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7M203/4-65 MIN.	IDT7M203/4-65 MAX.	IDT7M203/4-100 MIN.	IDT7M203/4-100 MAX.	IDT7M203/4-140 MIN.	IDT7M203/4-140 MAX.	UNIT	NOTES
t_{RC}	Read Cycle Time	85	—	125	—	165	—	ns	—
t_A	Access Time	—	65	—	100	—	140	ns	—
t_{RR}	Read Recovery Time	20	—	25	—	25	—	ns	—
t_{RRW}	Read Pulse Width	65	—	100	—	140	—	ns	2
t_{RLZ}	Read Pulse Low to Data Bus at Low Z	10	—	10	—	10	—	ns	3
t_{WLZ}	Write Pulse High to Data Bus at Low Z	15	—	20	—	20	—	ns	3
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	ns	—
t_{RHZ}	Read Pulse High to Data Bus at High Z	—	35	—	40	—	50	ns	3
t_{WC}	Write Cycle Time	85	—	125	—	165	—	ns	—
t_{WPW}	Write Pulse Width	65	—	100	—	140	—	ns	2
t_{WR}	Write Recovery Time	20	—	25	—	25	—	ns	—
t_{DS}	Data Setup Time	40	—	50	—	50	—	ns	—
t_{DH}	Data Hold Time	10	—	10	—	10	—	ns	—
t_{RSC}	Reset Cycle Time	85	—	125	—	165	—	ns	—
t_{RS}	Reset Pulse Width	65	—	100	—	140	—	ns	2
t_{RSR}	Reset Recovery Time	20	—	25	—	25	—	ns	—
t_{EFL}	Reset to Empty Flag Low	—	85	—	125	—	165	ns	—
t_{REF}	Read Low to Empty Flag Low	—	60	—	95	—	135	ns	—
t_{RFF}	Read High to Full Flag High	—	60	—	95	—	135	ns	—
t_{WEF}	Write High to Empty Flag High	—	60	—	95	—	135	ns	—
t_{WFF}	Write Low to Full Flag Low	—	60	—	95	—	135	ns	—

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1



*Includes jig and scope capacitances.

Figure 1. Output Load.

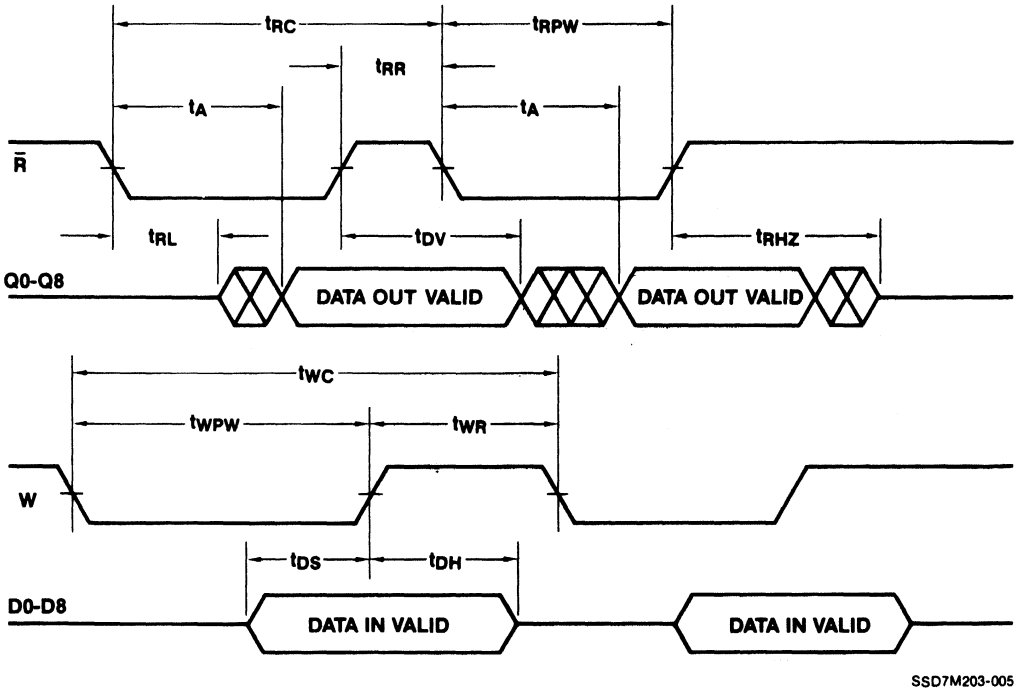


Figure 3. Asynchronous Write and Read Operation

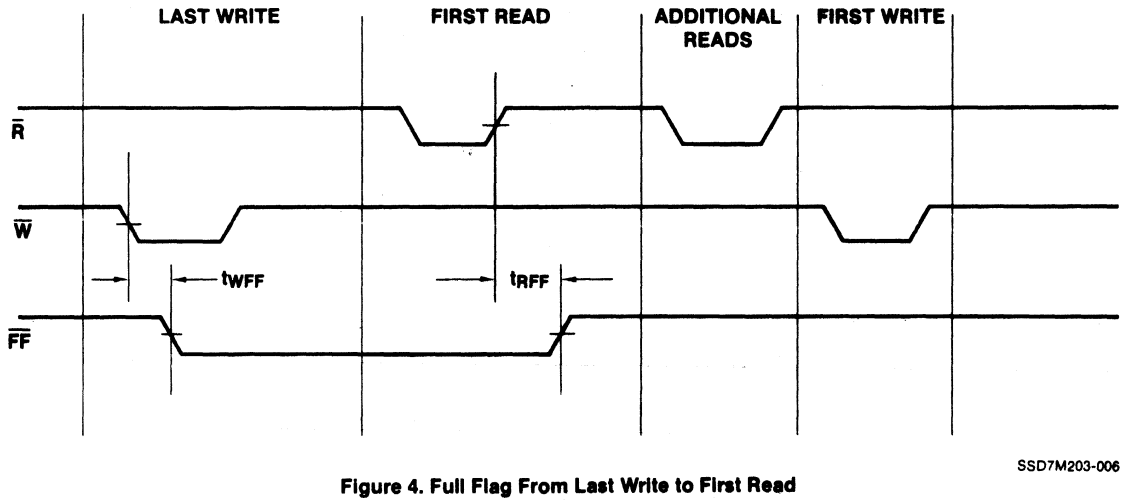


Figure 4. Full Flag From Last Write to First Read

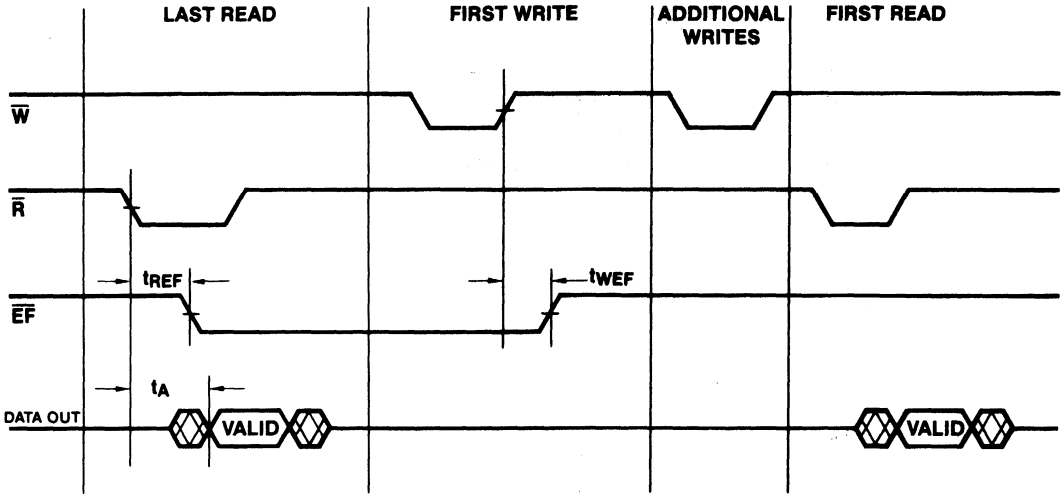
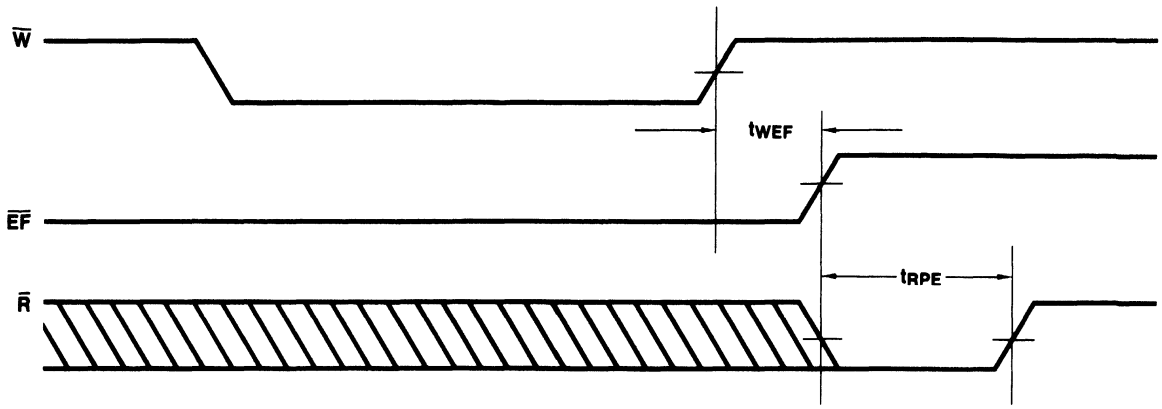


Figure 5. Empty Flag From Last Read to First Write

SUBSYSTEMS

t_{RPE}: EFFECTIVE READ PULSE WIDTH AFTER FULL FLAG HIGH

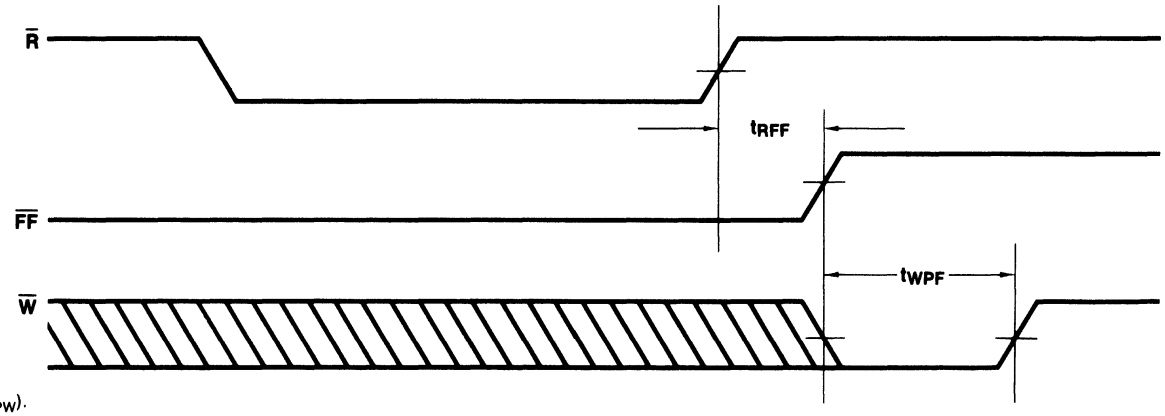


NOTE:
1. ($t_{RPE} = t_{RPW}$)

SSD7M203-008

Figure 6. Empty Flag Timing

t_{WPF}: EFFECTIVE WRITE PULSE WIDTH AFTER FULL FLAG HIGH



NOTE:
1. ($t_{WPF} = t_{WPW}$).

SSD7M203-009

Figure 7. Full Flag Timing

TRUTH TABLES

TABLE I — RESET — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

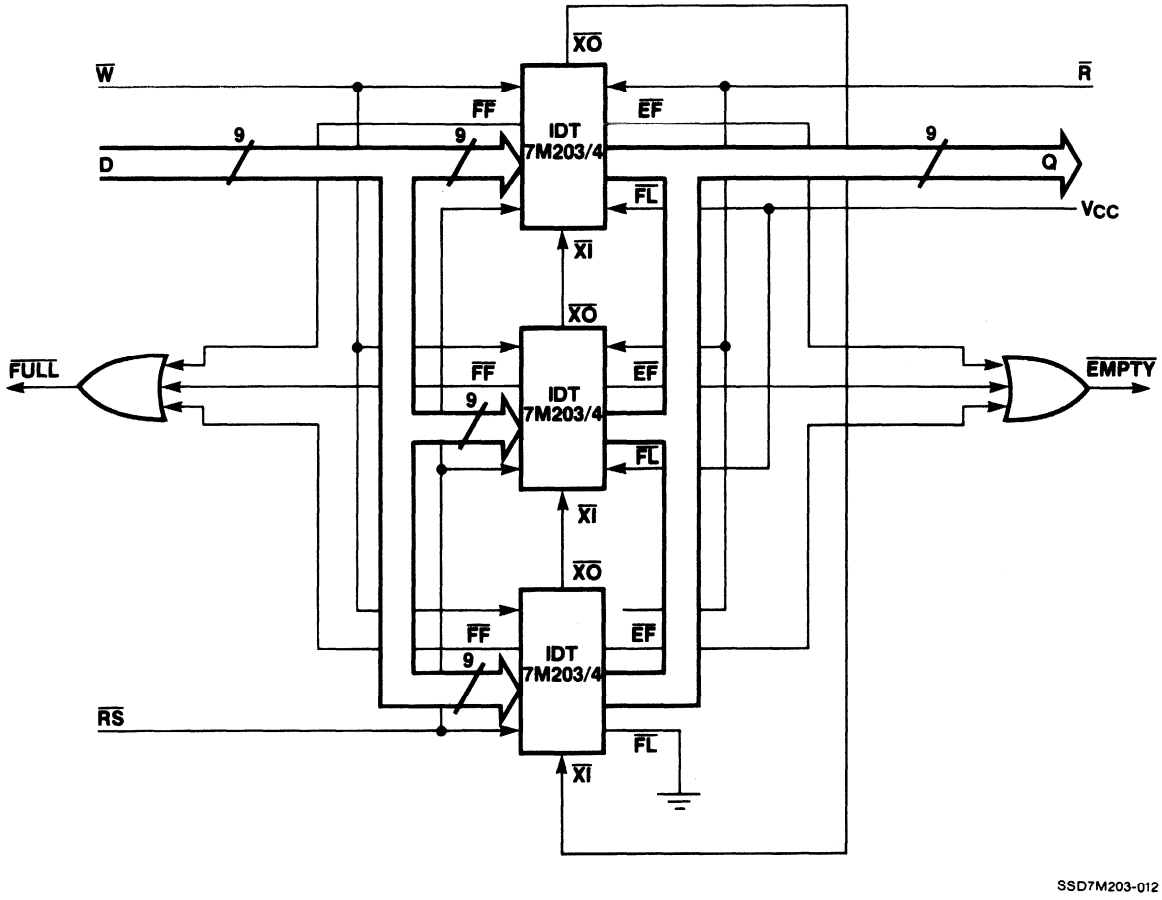
MODE	INPUTS		INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset	0	0	Location Zero	Location Zero	0	1
Read/Write	1	0	Increment(1)	Increment(1)	X	X

NOTE:
1. Pointer will increment if flag is high.

TABLE II — RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

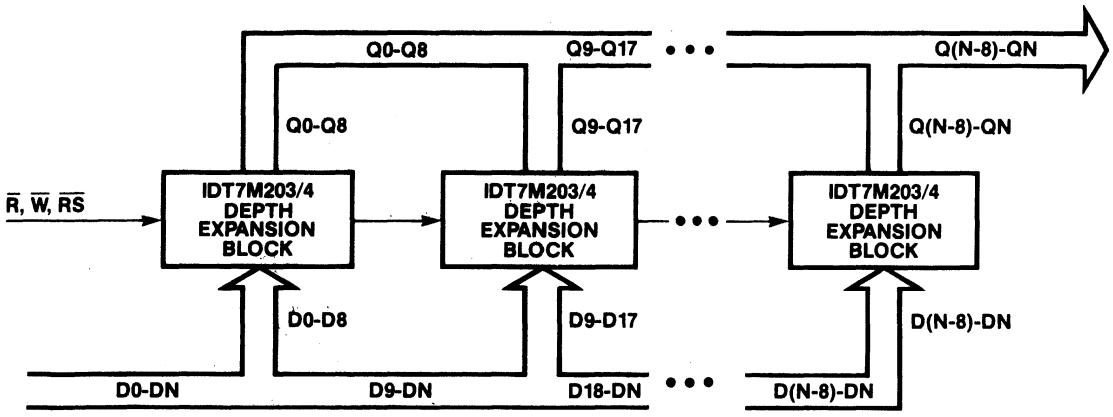
NOTES:
1. $\overline{XI}$ is connected to $\overline{Xo}$ of previous device. See Figure 10.
   $\overline{RS}$ = Reset Input, $\overline{FL}$ = First Load, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.



SSD7M203-012

Figure 10. Block Diagram of 6144x9/12288x9 FIFO Memory (Depth Expansion)

SUBSYSTEMS



NOTES:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 10.
2. For Flag detection see WIDTH EXPANSION Section and Figure 9.

Figure 11. Compound FIFO Expansion

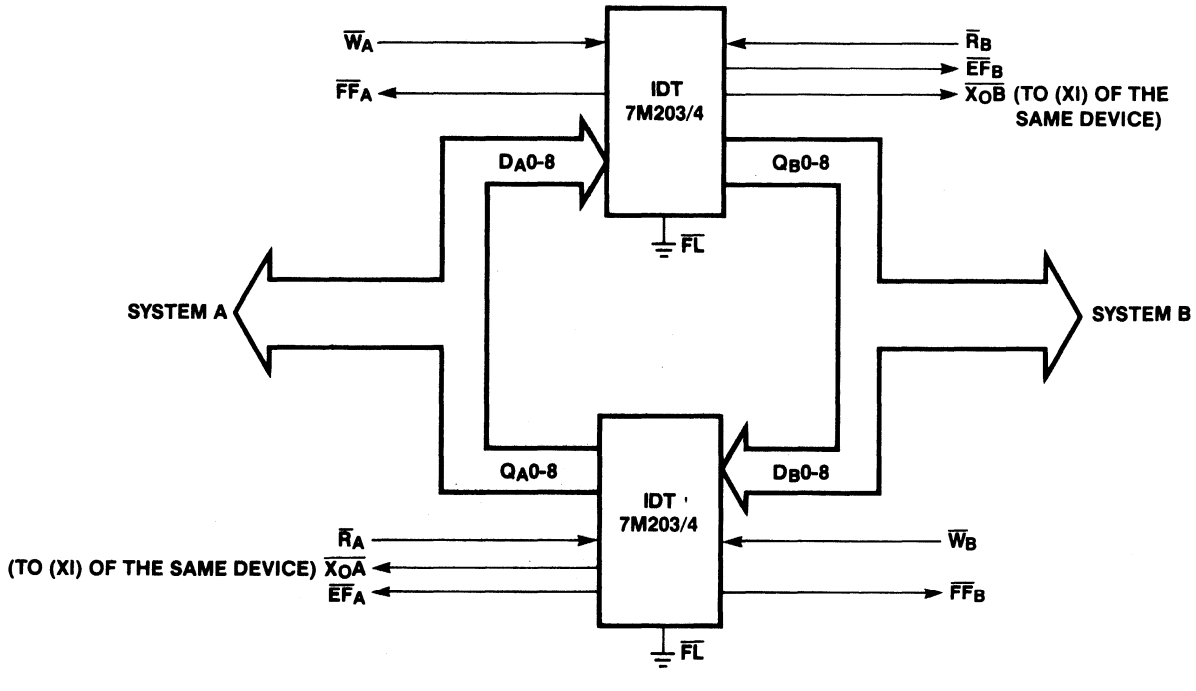


Figure 12. Bidirectional FIFO Mode

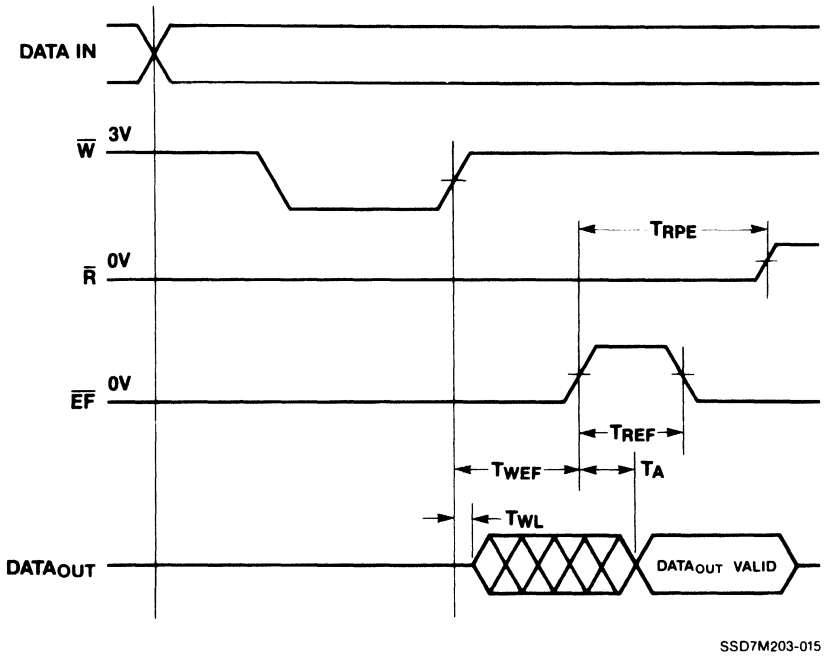


Figure 13. Read Data Flow-Through Mode

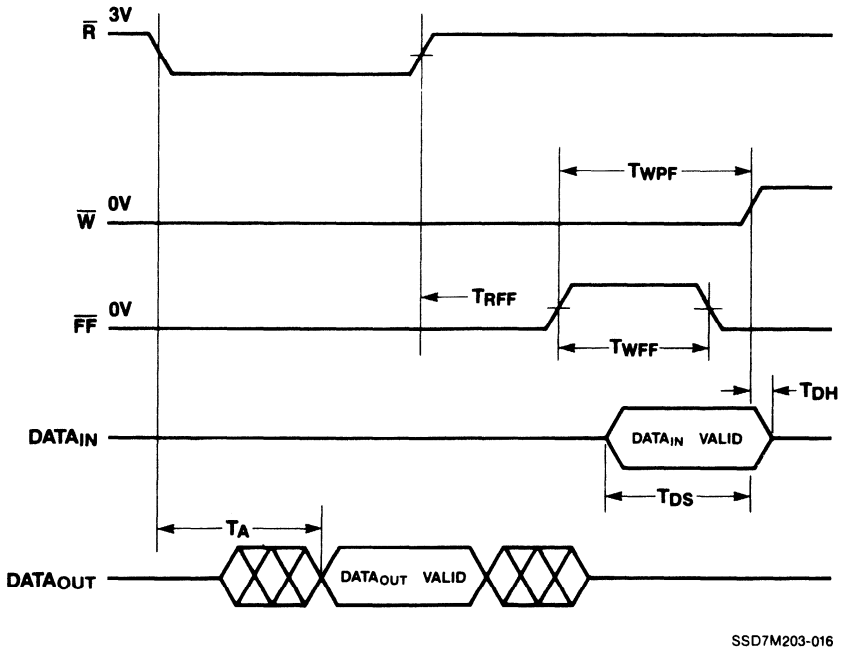


Figure 14. Write Data Flow-Through Mode

SUBSYSTEMS

GENERAL INFORMATION

CONTENTS **PAGE**

IDT PROCESSING SUMMARY

Maintaining the highest standards of quality in our monolithic hermetic products is the basis of IDT's standard manufacturing systems and procedures. IDT products begin with stringent design rules derived for use in high reliability programs.

This is followed by a dedicated commitment to reliable workmanship as well as rigid controls throughout wafer fab, device assembly and electrical test, all of which are designed to produce products that are inherently reliable.

All military grade monolithic products are manufactured and screened to the demanding requirements of MIL-STD-883, Method 5004, Class B. Standard grade products differ from military grade only in burn-in time and electrical test temperature. The military grade processing includes 100% 160-hour burn-in at T_A = +125°C (or equivalent) per Method 1015 followed by 100% temperature testing of all DC and AC parameters and DC functional characteristics over the full -55°C to +125°C temperature range.

For module assemblies, additional screening of the fully assembled RAMPAKs is performed per Figure 3 to assure package integrity and mechanical reliability. Finally, 100% electrical tests are performed.

Samples of the monolithic product which have been processed to Method 5004 100% screening requirements are submitted to the Quality Conformance inspection requirements of MIL-STD-883. These Quality Conformance inspections, as shown in Figure 2, are performed to the criteria of Method 5005, Group A (electrical), Group B (mechanical), Group C (chip integrity), and Group D (package environmental integrity).

For special customer specifications or quality requirements beyond Class B levels of MIL-STD-883 – such as SEM analysis, X-ray, or other screening flows to meet specific needs – contact your local IDT sales office.

MONOLITHIC COMPONENT SCREENING FLOW

SCREEN	TEST METHOD	LEVEL
Visual and Mechanical		
Internal visual	2010 Condition B	100%
High-temperature storage	1008 Condition C	100%
Temperature cycle	1010 Condition C	100%
Constant acceleration	2001 Condition E (Y_1 only)	100%
Hermeticity	1014	
Fine	Condition A or B	100%
Gross	Condition C	100%
Burn-In		
Pre-burn-in electrical	Per applicable device specifications at T_A = +25°C	100%
Burn-in	MIL-STD-883 Grade Product Method 1015, Condition D	100%
	Standard Grade Product 48 hours minimum to same burn-in conditions as Military Grade Product	100%
Final Electrical Tests (see Note 1)	5004	
Static (dc)	a) @ T_A = +25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A = +25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A = +25°C, nominal power supply	100%
Percent Defective Allowable (PDA)	Method 5004	
Calculated at post burn-in at T_A = +25°C	Military Grade	5%
	Standard Grade	10%
Quality Conformance	5005 Sample selection as applicable	Sample
External Visual	2009 Per IDT or customer specification	100%

Note 1:
Standard Grade Products are sample tested to the applicable temperature extremes.

Fig. 1

QUALITY CONFORMANCE TESTING PER MIL-STD-883, METHOD 5005, CLASS B

SCREEN	TEST METHOD	LEVEL
Quality Conformance Sample Tests	Group A (Electrical Tests)	Sample
	Group B (Mechanical Tests)	Sample
	Group C (Chip Integrity Tests)	Sample
	Group D (Package Integrity Tests)	Sample

Fig. 2

FULLY ASSEMBLED MODULE SCREENING FLOW

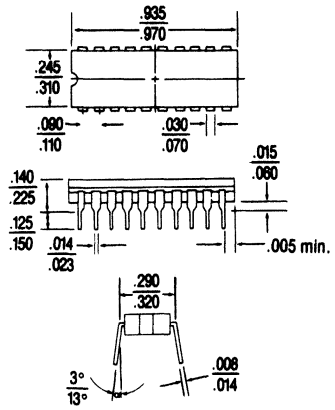
SCREEN	TEST METHOD	LEVEL
Burn-in	MIL-STD-883 Grade Product 48 hr. Method 1015, Condition D	100%
Final Electrical Tests Static (DC)	a. At 25°C and Power Supply Extremes	100%
	b. At Temperature and Power Supply Extremes	100%
Functional	a. At 25°C and Power Supply Extremes	100%
	b. At Temperature and Power Supply Extremes (IDT imposed)	100%
Switching (AC) or Dynamic	a. At 25°C and Power Supply Extremes	100%
	b. At Temperature and Power Supply Extremes (IDT imposed)	100%
External Visual	2009	100%

Fig. 3

PACKAGE OUTLINE DIAGRAMS

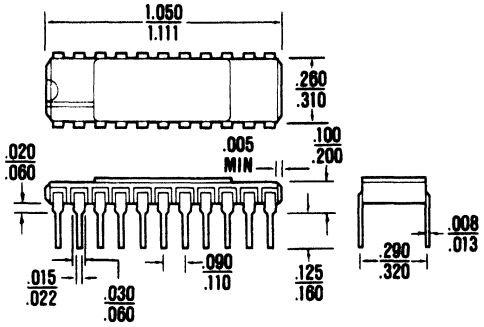
STATIC RAM PACKAGING

20-PIN CERDIP



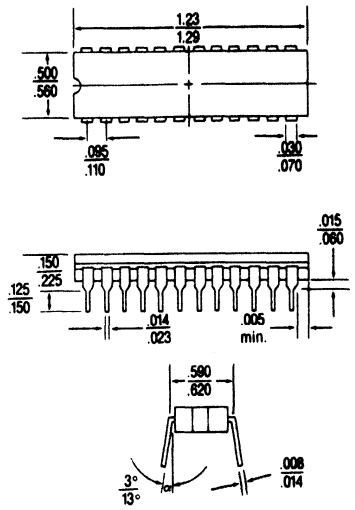
IDT6167
IDT6168

22-PIN SIDEBRAZE DIP



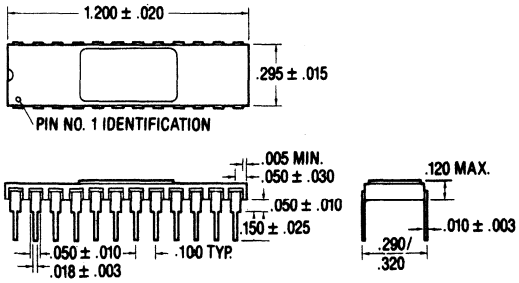
IDT7187
IDT7188

24-PIN CERDIP (600 MILS)



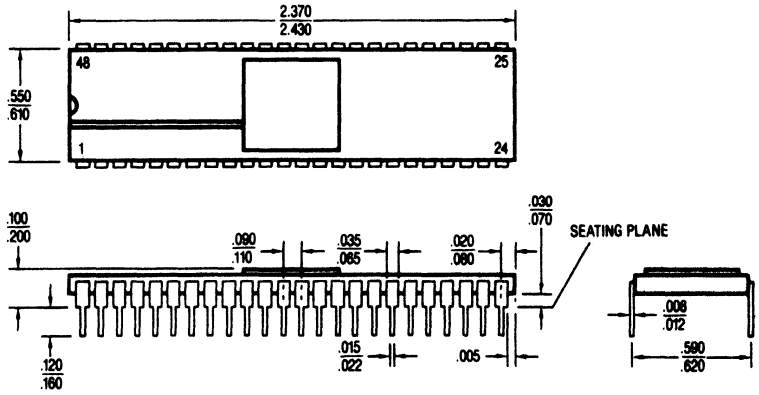
IDT6116

24-PIN SIDEBRAZE THIN DIP (300 MILS)



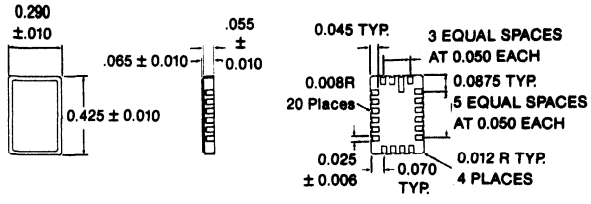
IDT6116
IDT71681
IDT71682

48-PIN SIDEBRAZE DIP



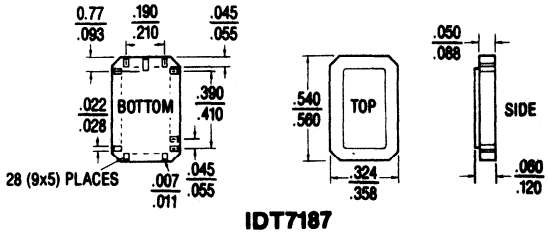
IDT7130
IDT7132

20-PIN LEADLESS CHIP CARRIER



IDT6167
IDT6168

28-PIN LEADLESS CHIP CARRIER (350 x 550 MILS)



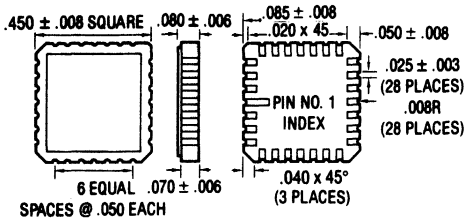
IDT7187
IDT7188

GENERAL

PACKAGE OUTLINE DIAGRAMS

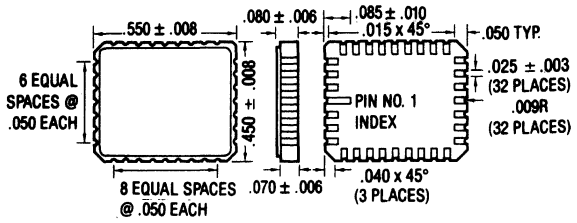
STATIC RAM PACKAGING (Continued)

28-PIN LEADLESS CHIP CARRIER (450 MILS²)



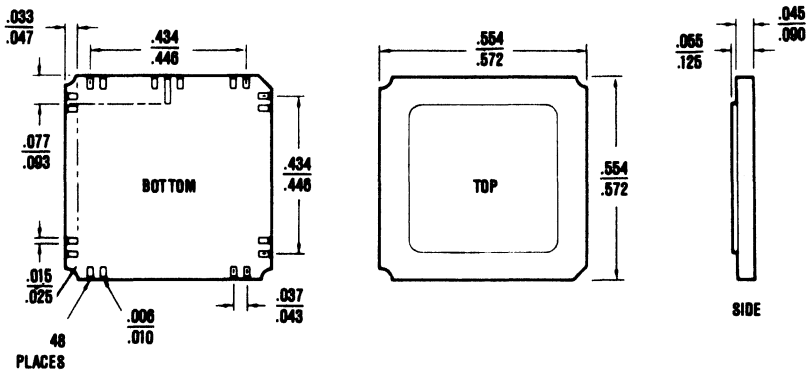
IDT6116
IDT71681
IDT71682

32-PIN LEADLESS CHIP CARRIER



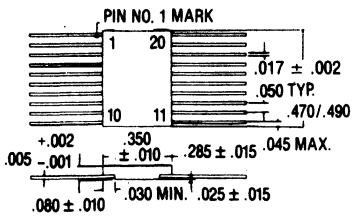
IDT 6116

48-PIN LEADLESS CHIP CARRIER



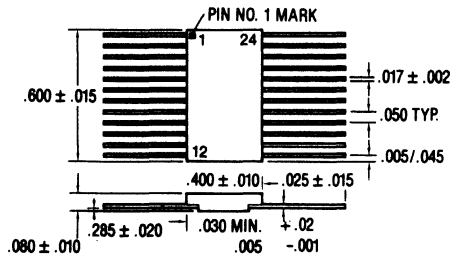
IDT7130
IDT7132

20-LEAD FLATPACK



IDT6167
IDT6168

24-LEAD FLATPACK

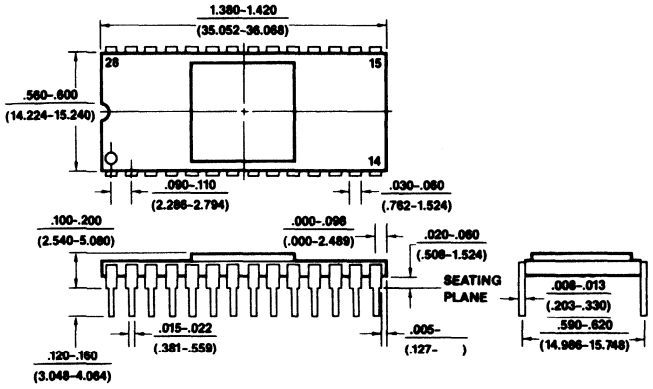


IDT6116
IDT71681
IDT71682

PACKAGE OUTLINE DIAGRAMS

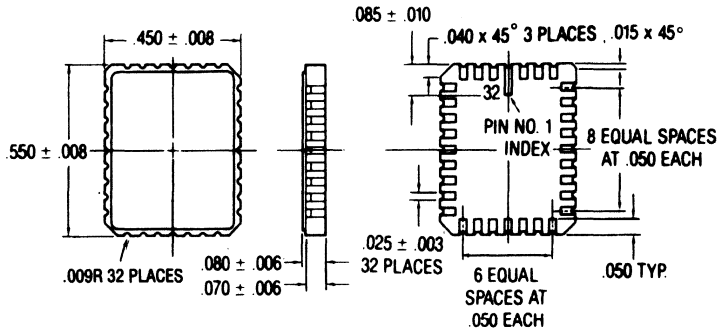
DSP PACKAGING

28-PIN SIDEBRAZE DIP



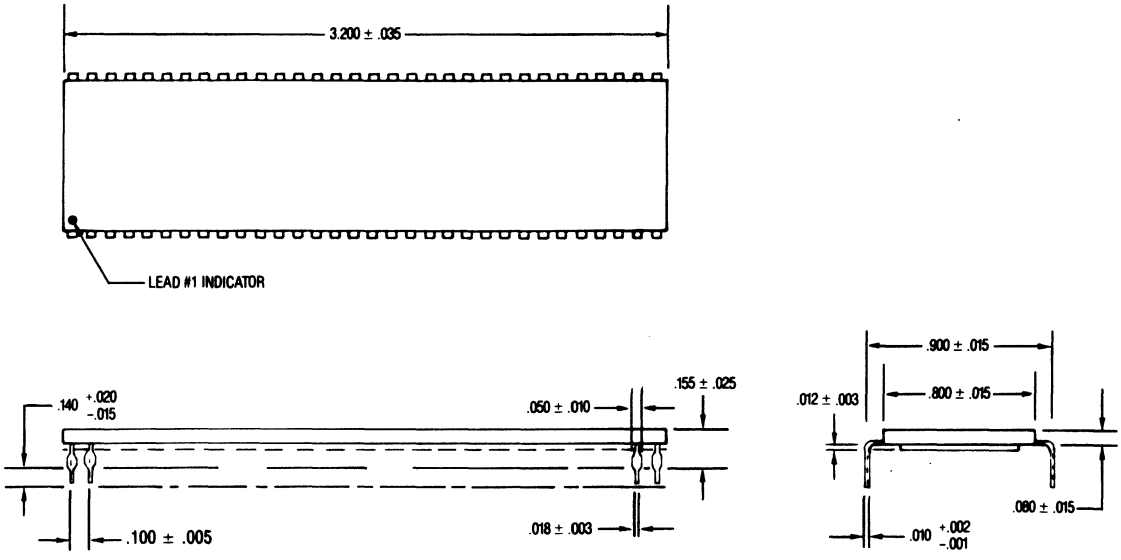
IDT7201/7202

32-PIN LEADLESS CHIP CARRIER



IDT7201/7202

64-PIN TOPBRAZE DIP



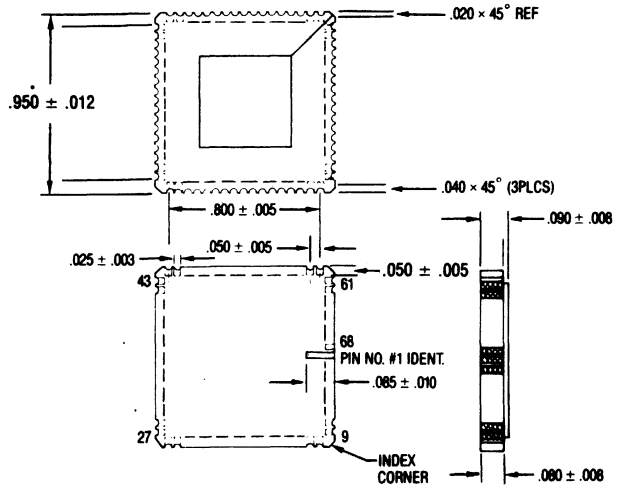
IDT7216/7217
IDT7212/7213
IDT7210/7243
IDT7209

GENERAL

PACKAGE OUTLINE DIAGRAMS

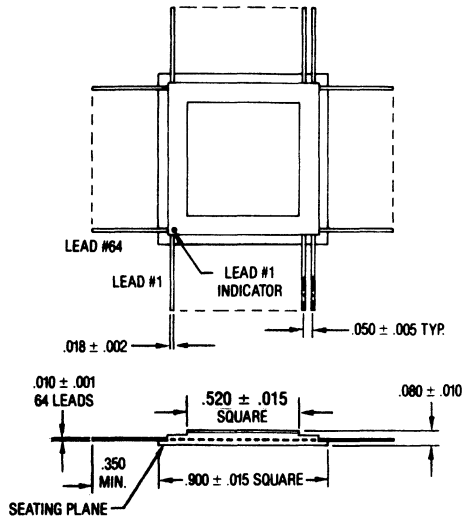
DSP PACKAGING (Continued)

68-PIN LEADLESS CHIP CARRIER



IDT7216/7217
IDT7212/7213
IDT7210/7243
IDT7209

64-LEAD FLATPAK

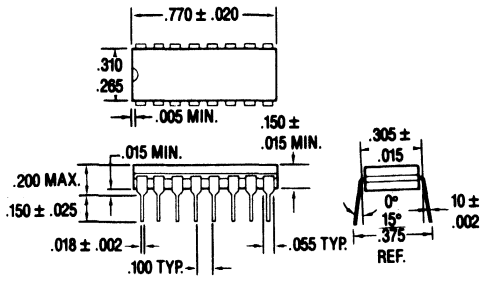


IDT7216/7217
IDT7212/7213

PACKAGE OUTLINE DIAGRAMS

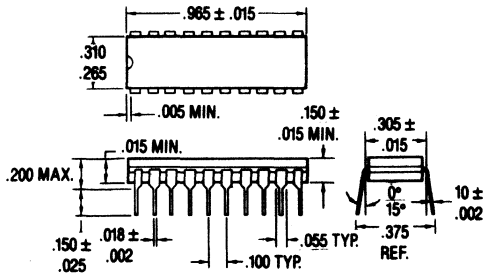
MEMORY INTERFACE LOGIC PACKAGING

16-PIN CERDIP



IDT54/74FCT138
IDT54/74FCT139
IDT54/74AHCT138
IDT54/74AHCT139

20-PIN CERDIP



IDT54/74FCT182
IDT54/74FCT240
IDT54/74FCT244
IDT54/74FCT245
IDT54/74FCT273
IDT54/74FCT299
IDT54/74FCT373
IDT54/74FCT374
IDT54/74FCT377
IDT54/74FCT521
IDT54/74FCT533
IDT54/74FCT534

IDT54/74FCT640
IDT54/74FCT645
IDT54/74AHCT182
IDT54/74AHCT240
IDT54/74AHCT244
IDT54/74AHCT245
IDT54/74AHCT273
IDT54/74AHCT299
IDT54/74AHCT373
IDT54/74AHCT374
IDT54/74AHCT377
IDT54/74AHCT521
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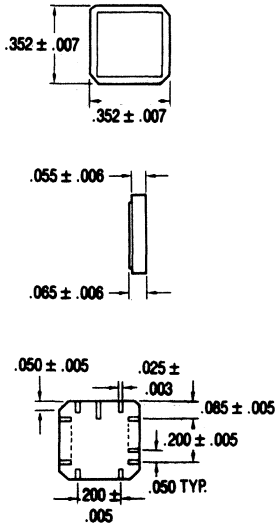
IDT54/74AHCT645

20-PIN LEADLESS CHIP CARRIER



IDT54/74FCT138
IDT54/74FCT139
IDT54/74AHCT138
IDT54/74AHCT139
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IDT54/74FCT240
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IDT54/74FCT245
IDT54/74FCT273
IDT54/74FCT299
IDT54/74FCT373
IDT54/74FCT374
IDT54/74FCT377
IDT54/74FCT521
IDT54/74FCT533
IDT54/74FCT534

IDT54/74FCT640
IDT54/74FCT645
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IDT54/74AHCT244
IDT54/74AHCT245
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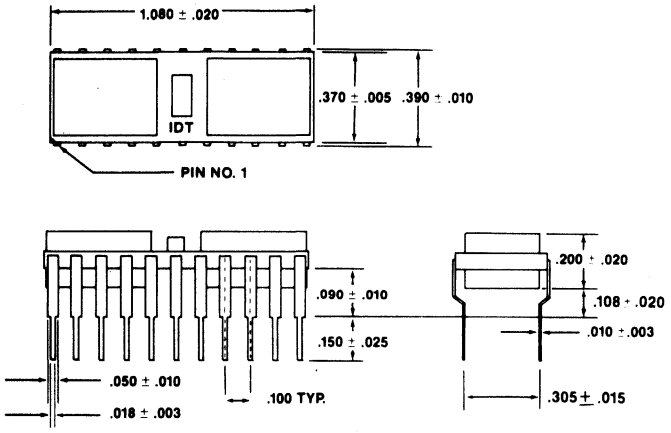
IDT54/74AHCT377
IDT54/74AHCT521
IDT54/74AHCT533
IDT54/74AHCT534
IDT54/74AHCT640
IDT54/74AHCT645

PACKAGE OUTLINE DIAGRAMS

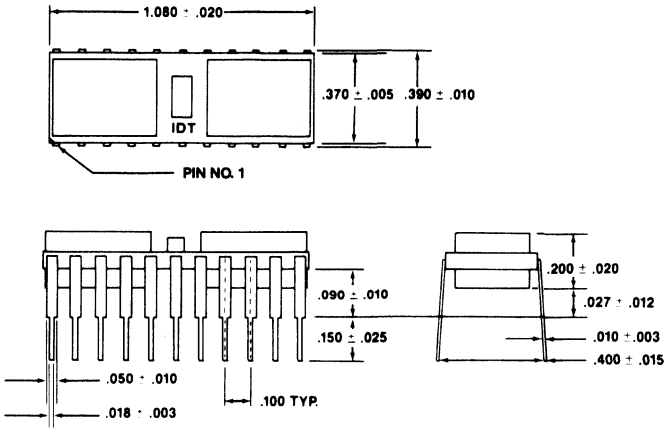
SUBSYSTEMS PACKAGING

22-PIN SIDEBRAZE DIP (300 MILS)



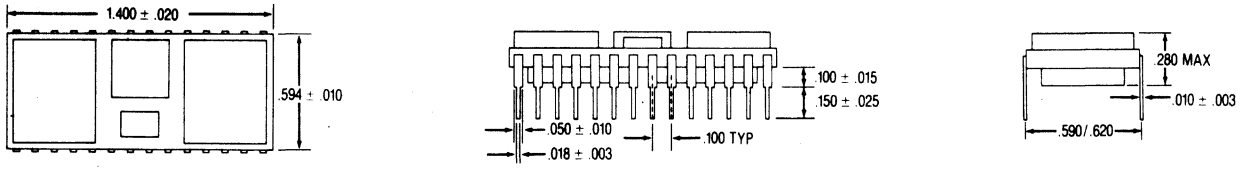
IDT7M164
IDT7M464

22-PIN SIDEBRAZE DIP (400 MILS)



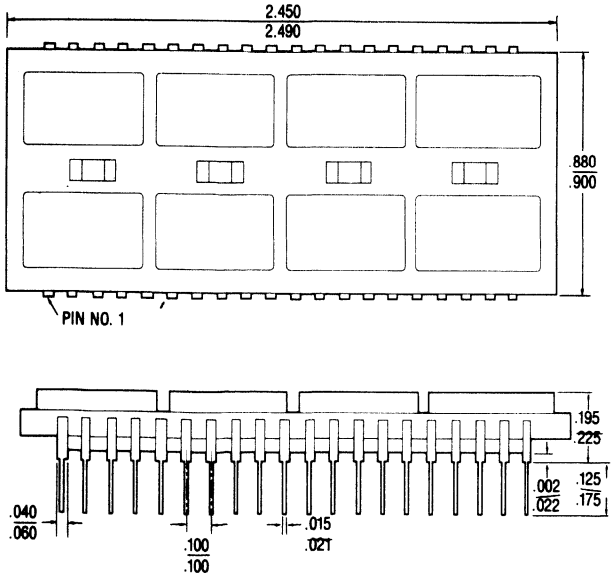
IDT8M464

28-PIN SIDEBRAZE DIP



IDT7M864 **IDT7M203**
IDT8M864 **IDT7M204**
IDT7M856

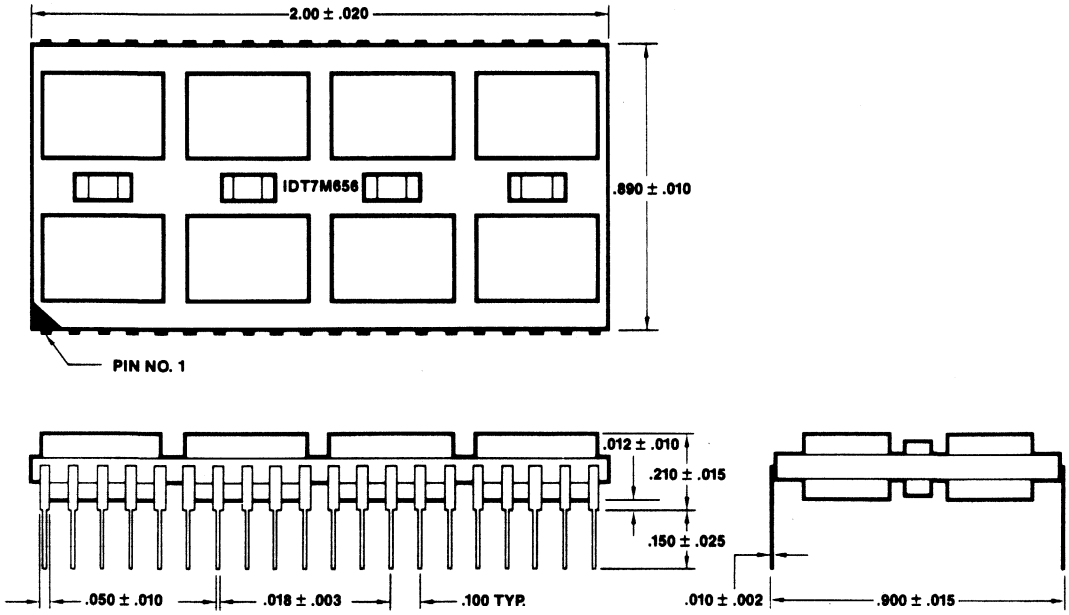
40-PIN SIDEBRAZE DIP



IDT7M624

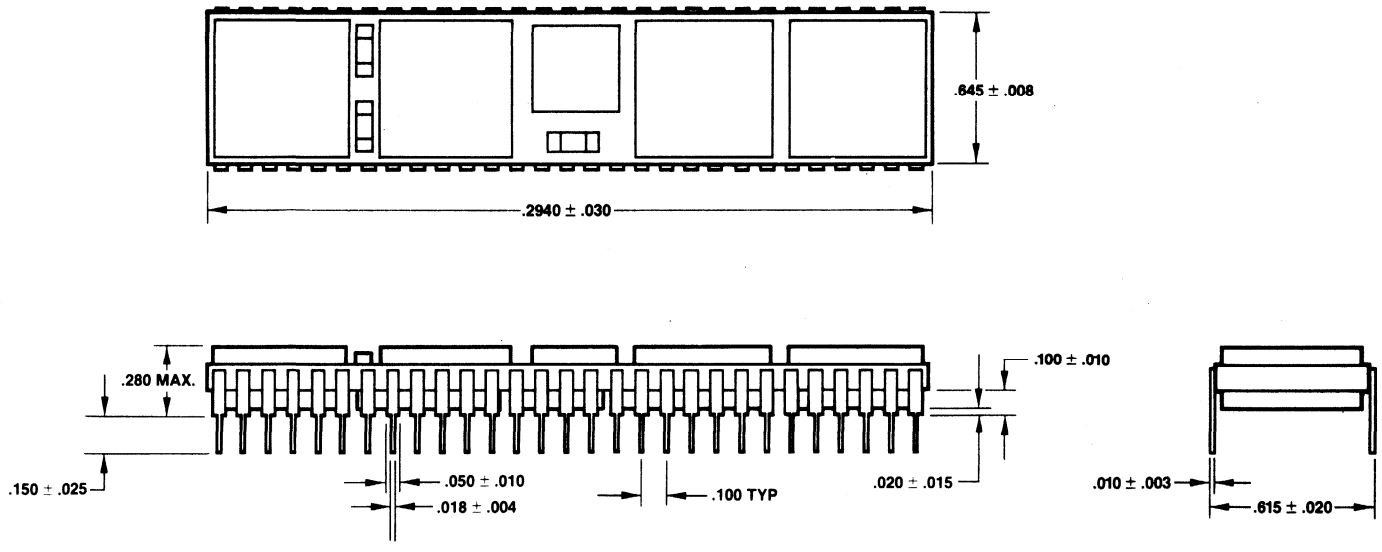
SUBSYSTEMS PACKAGING (Continued)

40-PIN SIDEBRAZE DIP



IDT7M656

58-PIN SIDEBRAZE DIP



7M134/135

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When ordering by TWX or Telex, the following format must be used:

A. Complete Bill To.
B. Complete Ship To.
C. Purchase Order Number.
D. Certificate of Conformance. Y or N
E. Customer Source Inspection. Y or N
F. Government Source Inspection. Y or N
G. Government Contract Number and Rating.
H. Requested Routing.
I. IDT Part Number —
   Each item ordered must use the complete part number exactly as listed in the price book.
J. SCD Number.
K. Customer Part Number/Drawing Number/ Revision Level—
   Specify whether part number is for reference only, mark only, or if extended processing to customer specification is required.
L. Customer General Specification Numbers/Other Referenced Drawing Numbers/Revision Levels.
M. Request Date With Exact Quantity.
N. Unit Price.
O. Special Instructions, Including Q.A. Clauses.

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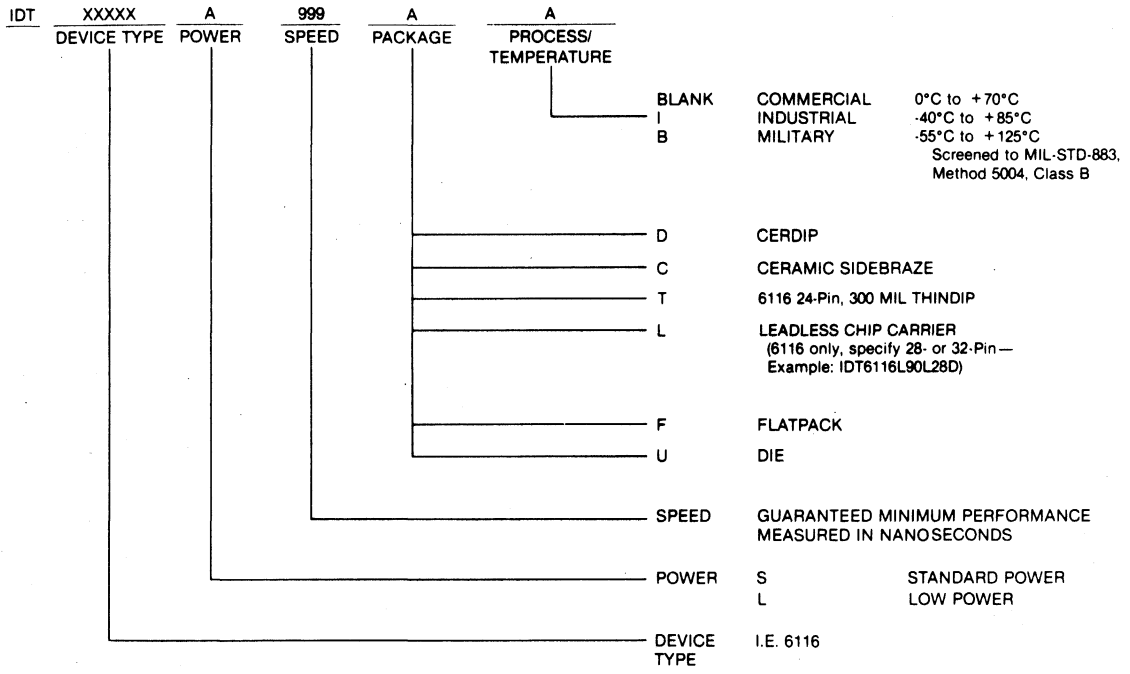
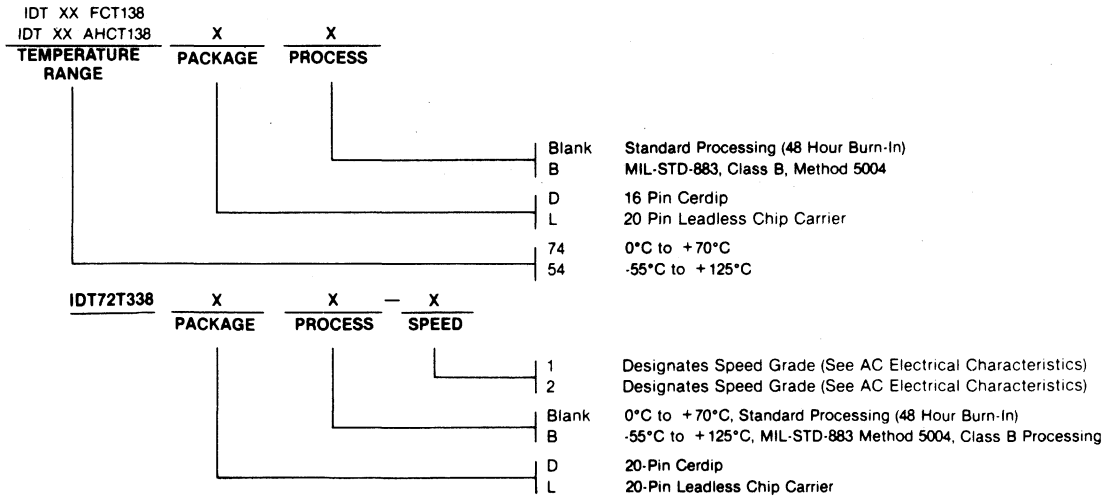
Dun & Bradstreet Number - 03-814-2600
Federal Tax I.D. - 94-2669985
TLX# - 887766
FAX# - 408-737-3468

Minimum Order Quantities:
OEM - $500.00
Distributor - $1,000.00
100 piece minimum on all Flatpack orders

ORDERING DESCRIPTION





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